Sri Muthukumaran Institute of Technology
Chikkarayapuram, Near Mangadu, Chennai – 600 069.
Academic Year 2023– 2024/ Odd Semester
Assessment Test I
Branch : ECE V sem
Subject Code : EC 3552
Subject Name : VLSI and Chip Design

UNIT I -MOS TRANSISTOR PRINCIPLES

PART A

1. **What are the two types of design rules?**
   - Micron rules
   - Lambda rules

2. **What is body effect ?**

   The resultant effect increases the channel substrate junction potential. This increases the rate-channel voltage drop. The overall effect is an increase in threshold voltage. This effort is called body effect.

3. **What is body effect coefficient?**

   The potential difference between the source and body affects the threshold voltage. The threshold voltage can be modeled as

   $Vt=Vt_0+\gamma((\Phi s+Vsb)^{1/2}-(\Phi s)^{1/2}$

   Where, Φs= surface potential at threshold γ= body effect coefficient

4. **What is the influence of voltage scaling on power and delay?**

   Constant voltage scaling increased the electric field in devices. By the 1μm generation velocity saturation was severe enough that decreasing feature size no longer improved device current. Aggressive process achieve delays in the short end of the range by building transistors with effective channel length.

5. **Determine whether an NMos transistor with a threshold voltage of 0.7v is operating in the saturation region if V_{gs}=2V and V_{ds}=3V.)**

   V_t=0.7 V_{gs}=2V V_d=3V
   NMos transistor is in saturation region if
   $V_{ds}>V_{gs}-V_t$
   3V >2V-0.7V
   3V > 1.3V
   It is in saturation region

6. **Write down the equation for describing the channel length modulation effect in NMos transistor.**
   - Ideally Ids is independent of V_{ds} insaturation.
   - The reverse biased p-n junction between the drain and body forms a depletion region with a width L_d that increases with V_{db}.

- The depletion region effectively shortens the channel length to $L_{eff} = L - L_d$.
- Imaginethatthesourcevoltageisclosetothebodyvoltage.IncreasingV_{ds} decreases the effective channel length.

$$I_{ds}=\beta(V_{gs}-V_t)^2/2$$

7. Write the expression for the logical effort and parasitic delay of an input NOR gate.

Logical effort of n input Nor gate

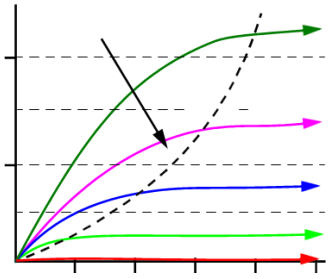
$$I_{ds} = \frac{(Vgs - V_t)2\ (1+\ V\ ds)}{2}$$

G=(2n+1)/3
N=number of inputs

8. Why does interconnect increase the circuit delay?

The wire capacitance adds loading to each gate. The long wire contributes RC delay or flight time. Circuit delay can be increased by interconnect

9. Draw the IV characteristics of Mos transistors.



10. Brief the different operating regions of Mos system.)

Different operating regions of Mos system

- Cut off or subthreshold region
- Linear or non-saturation region
- Saturation region

11. Why the tunneling current is higher for NMOS transistor than PMOS transistor with silica gate?

Tunneling current is an order of magnitude higher for nMOS than PMOS transistor with Sio_2 gate dielectrics because the electrons tunnel from the conduction band while the holes tunnel from the valance band.

12. What is the objective of layout rules?

Layout design rule is examined and a scale parameter lambda is n defined as the half width of a minimum width line or as a multiple of standard deviation of a process. Designing layouts in terms of lambda allows for future scaling makes the layout portable.v

13. What are the advantages of CMOS technology ?(May2013)

a. Low powerconsumption.
b. Highperformance.
c. Scalable thresholdvoltage.
d. High noisemargin.
e. Low output drivecurrent.

14. Compare NMOS and PMOS.

NMOS	PMOS
The majority carriers are electron	Themajoritycarriersareholes
Positive voltage is applied at the gate	Negative voltage is applied at the gate
tNeMrmOinSaconducts at logic1	tPeMrmOinSalconducts at logic0
Mobility of electron is high	Mobility of electron is low
Switching speed is high	Switching speed is low

15. What is latch up? How to prevent latch up? (MAY/JUN2016)

Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDD and VSS with disastrous results. Careful control during fabrication is necessary to avoid this problem.

16. *Why nMOS transistor is selected as pull down transistor.*(Nov/Dec-17)

When high voltage is given at the input nMOS is turned ON. So the output is pulled down to Vss. An NMOS device pulls the output all the way down to GND,while a PMOS lowers the output no further than |VTp|—thePMOSturnsoffatthatpoint,andstopscontributingdis-chargecurrent.NMOStransistorsarehence the preferred devices in the PDN.

17.

Define propagation delay of CMOS Inverter. *(Apr/May-17)*

The inverter propagation delay (t_P) is defined as the average of the low-to-high (t_{PLH}) and the high-to low (t_{PHL}) propagation delays: $t_p = \frac{t_{PHL} + t_{PLH}}{2}$.

Propagation delays t_{PLH} and t_{PHL} are defined as the times required for output voltage to reach the middle between the low and high logic levels, i.e. 50 % of V_{DD} in our case of CMOS logic.

18. Define Threshold voltage in CMOS.

The Threshold voltage, V_T for a MOS transistor can be defined as the voltage applied between

the gate and the source of the MOS transistor below which the drain to source current, IDS effectively drops to zero.

9. Define any two layout design rules. ***(Nov/Dec-15, May/Jun-14)***

Micron design rule:

Micron rules specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers.

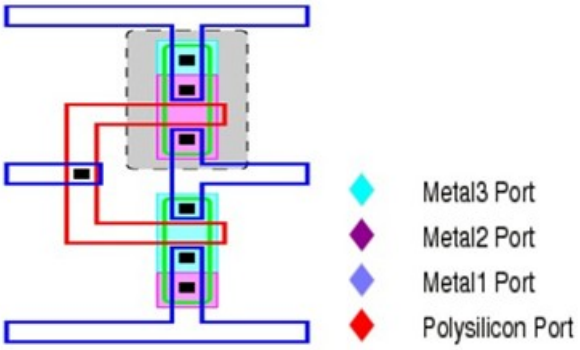
Lambda design rule:

Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

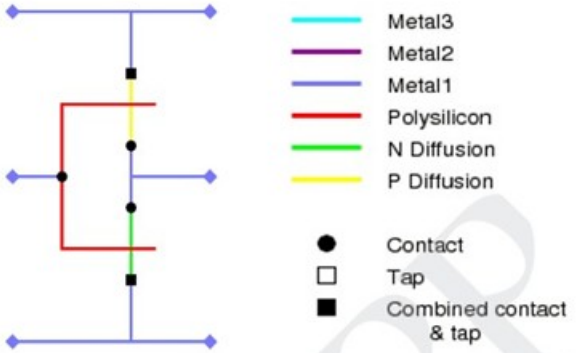
20.

Draw the stick diagram and layout for CMOS Inverter. ***(Nov/Dec-16)***

Layout for CMOS Inverter:



Stick diagram for CMOS Inverter:

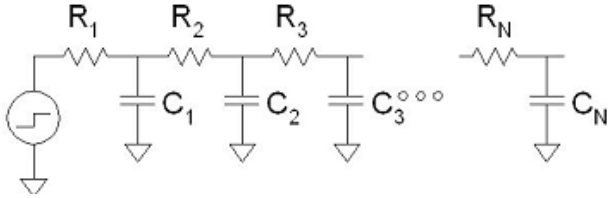


21.**What is Elmore's Constant? Give Elmore delay expression for propagation delay of an inverter.**

It is an analytical method used to estimate the RC delay in a network.Elmore delay model estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance Rn-1 between that node and a supply multiplied by the capacitor on the nodes.

$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

$$= R_1 C_1 + (R_1 + R_2) C_2 + \ldots + (R_1 + R_2 + \ldots + R_N) C_N$$

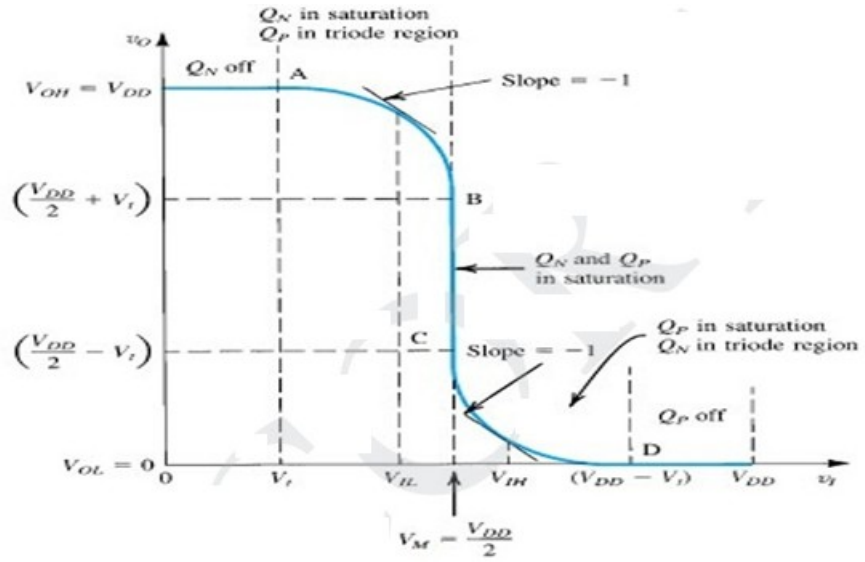


22.State the advantages of transmission gate.*(Apr/may-17)*

- Multiplexing element of path selector

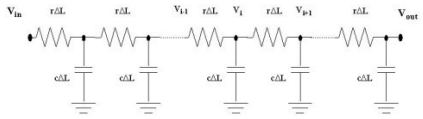
- A latch element
- A nun lock switch
- Act as a voltage controlled resistor connecting the input and output.

23.Draw the DC transfer characteristics of CMOS inverter.



24.Give the expression for Elmore delay and state the various parameters associated with it.

Viewing on transistors as resistors a chain of transistors as an RC ladder. The Elmore model estimates the delay of an RC ladder as the sum over each node in the ladder of the resistance between that node and a supply multiplied by the capacitance on the node.



$$\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$$

25. Give the various color coding used in stick diagram.

- Green – n-diffusion
- Red- polysilicon
- Blue –metal
- Yellow- implant

PART-B

1. **Discuss in detail about the working operation of MOSFET transistor and its mode of operation with neat sketches.(MAY'11)**

NMos transistors are built on a p-type substrate of moderate doping. Source and drain are formed by diffusing heavily doped n-type impurities (n+) adjacent to the gate. A layer of silicon dioxide (SiO_2) or glass is place over the substrate in between the source and drain. Over SiO_2, a layer of polycrystalline silicon or polysilicon is formed, from which the gate terminal istaken.

The following figure shows the structure and symbol of nMOS transistor.

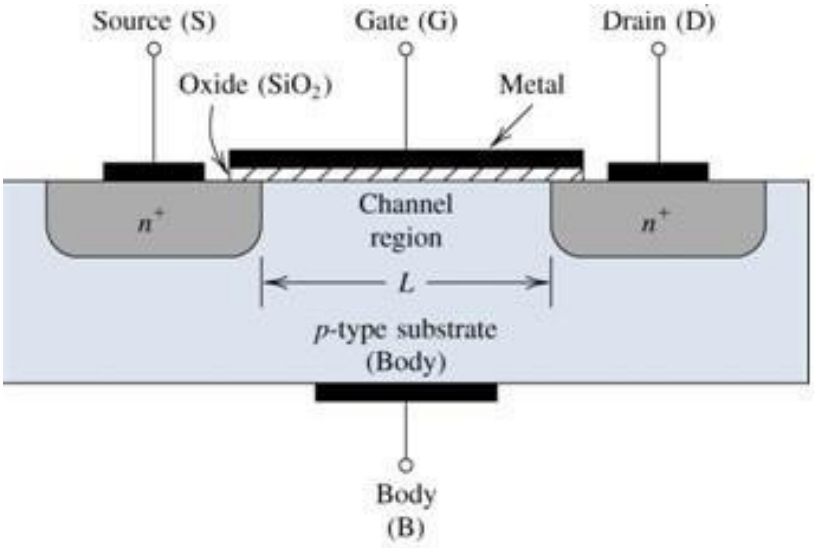


Fig: nMOS transistor.

Threshold Voltage (V_t)

It can be defined as the voltage applied between the gate and the source of a MOSdevice (V_{gs}) below which the drain-to-source current (I_{ds}) "effectively" drops to zero. V_t depends on the following:

- Gate conductionmaterial
- Gate insulationmaterial
- Gate insulatorthickness
- Channeldoping
- Impurities at the silicon-insulator interface
- Voltage between the source and the substrate,V_{sb}.

Modes of operation of MOS Transistor:

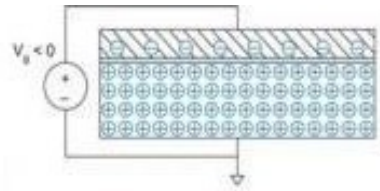
The following are the three modes of operation of nMOS transistor:

1. Accumulation mode
2. Depletion mode

3. Inversion mode

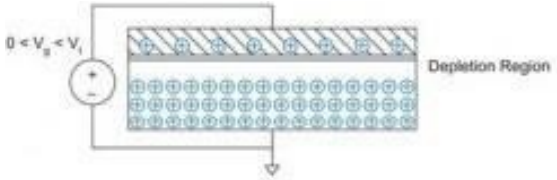
a. AccumulationMode

In this mode a negative voltage is applied to the gate. So there is negative charge on the gate. The mobile positively charged holes are attracted to the region beneath the gate.



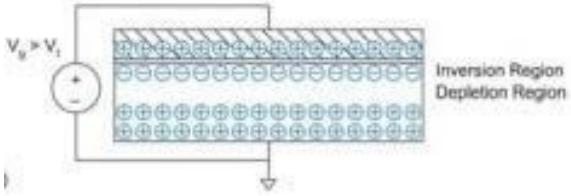
b. DepletionMode:

In this mode a low positive voltage is applied to the gate. This results in some positive charge on the gate. The holes in the body are repelled from the region directly beneath the gate.



c. InversionMode:

In this mode, a higher positive potential exceeding a critical threshold voltage is applied. This attracts more positive charge to the gate. The holes are repelled further and a small number of free electrons in the body are attracted to the region beneath the gate. This conductive layer of electrons in the p-type body is called the inversion layer.



Behavior of nMOS with different voltages:

The Behavior of nMOS with different voltages can be classified into the following three cases and is illustrated in below figure.

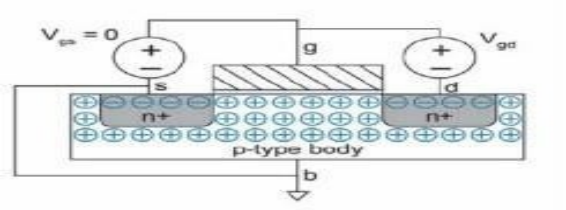
i. Cut-off region

ii. Linear region

iii. Saturation region

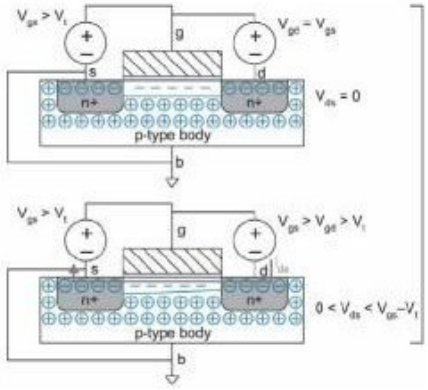
a. Cut-offregion:-

In this region $V_{gs}<V_t$ .The source and drain have free electrons. The body has free holes but no free electrons. The junction between the body and the source or drain is reverse biased. So no current will flow. This mode of operation is called cut-off.



Linear region:-

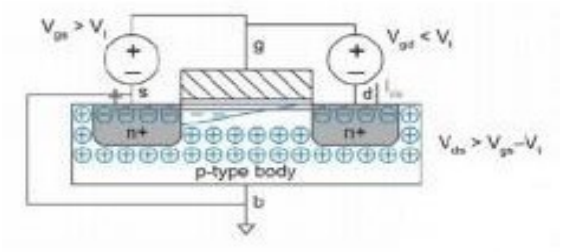
In this region $V_{gs}>V_t$ .Now an inversion region of electrons called the channel connects the source and drain. This creates a conductive path between source and drain. The number of carriers and the conductivity increases with the gate voltage. The potential difference between drain and source is $V_{ds} = V_{gs} – V_{gd}$. If $V_{ds}=0$,there is no electric field tending



to push current from drain to source.

b. Saturation region:-

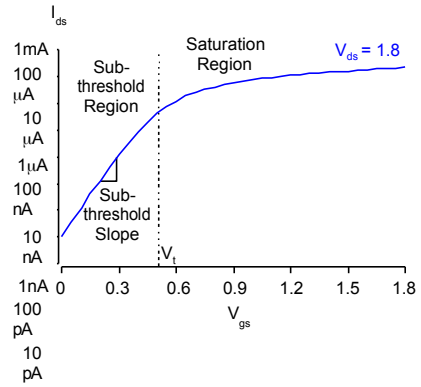
In this region V_{ds} becomes sufficiently larger than $V_{gd}< V_t$, the channel is no longer inverted near the drain and becomes pinched off .Above this drain voltage, the I_{ds} is controlled only by the gate voltage. This mode is called saturation mode.



2. Explain in detail about Non-ideal I-V characeteristics of p-MoS and n-MoS Transistors (MAY/JUN 2016)

Non- Ideal I-V Effects:

The I_{ds} value of an ideal I- v model neglects many effects that are important to modern devices.



Simulated I-V Characteristics

- While compared to the ideal devices, the saturation current increasesless than a quarter with increasing V_{gs}. This is caused by twoeffects.
  1) VelocitySaturation
  2) Mobilitydegradation.
- At high lateral field strengths V_{ds} . carrier velocity ceases to increase L linearly with field strength. This is called velocity saturation and this results in lesser I_{ds} than expected at high V_{ds}.
- Current between source and drain is the total amount of charge in the channel divide the time required to crossit.

$I_{ds} = Q_{Channel}$

By Sub the values we get

$I_{ds} = \frac{W}{} (V_{gs} - V_t - V_{ds}) V_{ds}$

$Ids = (V_{gs} - V_t - \frac{V_{ds}}{}) V_{ds}$

In linear region $V_{gs} > V_t$ and V_{ds} is relatively small.

Saturation Region:-

- In saturation region , if $V_{ds} > V_{dsat}$, the channel is pinched off. ie; $V_{ds} = V_{gs} - V_t$

Beyond this point it is often called the drain saturation voltage.

In saturation, I_{dsat} is

$V_{gs} = V_{ds} + V_{DD}$

$I_{dsat} = (V_{DD} - V_t)^2$

Summarizing the three regions we get.

$$I_{ds} = \begin{cases} 0 & ; V_{gs} < -V_t \text{ ; cutoff} \\ (V_{gs} - V_t - \frac{V_{ds}}{2}) V_{ds} & ; V_{ds} < V_{dsat} \text{; linear} \\ \beta/2 (V_{gs} - V_t)^2 & ; V_{ds} > V_{dsat} \text{ ;saturation.} \end{cases}$$

- At high vertical field strengths V_{gs}/ tor the carrier scatlers more often. This is called mobility degradation and this leads to less current than expected at high V_{gs}
- The threshold voltage itself is influenced by the voltage difference between the source and body called the bodyeffect.

The non- ideal Iv effect include the following:-

1) Velocity saturation & mobilitydegradation.
2) Channel lengthmodulation
3) Bodyeffect
4) Sub thresholdcondition
5) JunctionLeakage
6) Tunneling
7) Temperaturedependence
8) GeometryDependence.

Velocity saturation and mobility degradation:-

- Carrier drift velocity and current increase linearly with the lateralfield E lat = V_{ds}/ L between source anddrain.
- At high field strength, drift velocity rot off due to carrier scatteringand eventually saturates at V_{sat}.
- Without velocity saturation the saturation currentis

$$I_{ds} = C_{ox} \frac{W}{L} \frac{(Vgs - V_{ds})^2}{2}$$

- If the transistor is completely Velou saturated V = V_{sat} and saturation currentbecome.

- $Ids = C_{ox} W (V_{gs} - V_t) V_{sat}$ without velocity saturation .

$$Ids = \begin{cases} 0 & ; V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat} = V_{ds} & ; V_{ds} < V_{dsat} \quad \text{linear } V_{dsat} \\ I_{dsat} & ; V_{ds} > V_{dsat} \quad \text{saturation.} \end{cases}$$

Where

$$I_{dsat} = P_c \frac{}{\beta} (V_{gs} - V_t)^2$$

$$V_{dsat} = P_v (V_{gs} - V_t)^2 \propto /2 .$$

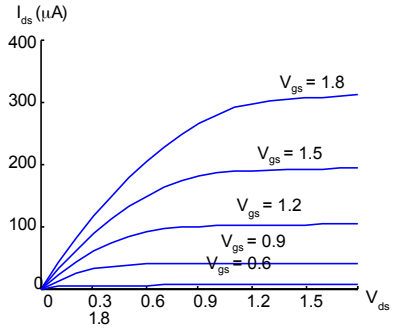
- As channel length becomes shorter, the lateral field increases and transistors become more velocity saturated, and the supply voltage is heldconstant.

Channel Length Modulation:-

- Ideally Ids is independent of V_{ds} insaturation.
- The reverse biased p-n junction between the drain and body forms a depletion region with a width L_d that increases with V_{db}.
- The depletion region effectively shortens the channel length to Leff=L-Ld.

- Imagine that the source voltage is close to the body voltage. Increasing V_{ds} decreases the effective channel length. Shorter length results in higher current. Thus I_{ds} increases with V_{ds} in saturation as shownbelow.

Where λ = Channel length modulation factor .



Body Effect:

Transistor has four terminals named gate, source, drain and body. The potential difference between the source and body V_{sb} affects the threshold voltage.

$$V_t = V_{to} + \delta \left(\sqrt{p_s + V_{sb}} - \sqrt{\varphi_s} \right)$$

Where

V_{to} = Threshold Voltage when the source is at the body potential

φ_s = Surface Potential at threshold = $2v_T \ln \frac{N_d}{N_i}$

V_{sb} = Potential difference between the source and body.

Sub threshold condition:

- Ideally current flows from source to drain when $V_{gs} > V_t$. In real transistor, current does not abrupthy cut off below threshold, but rather drops off exponentiallyas

$$I_{ds} = I_{dso} e^{\frac{V_{gs} - V_t}{nvt}} \left[1 - e^{\frac{V_{ds}}{V_t}} \right] .$$

This is also called as leakage and often thias results in underired current when a transistor is normally OFF. $I_{dso}$is the current at thresholo and is dependent on process and device geometry

Applications:-

- This is used in very low power analogcircui
- This is used in dynamic circuits and ORAM

Advantage:

1) Leakage increases exponentially as V_t decreases or as temperature rises.

Disadvantages:

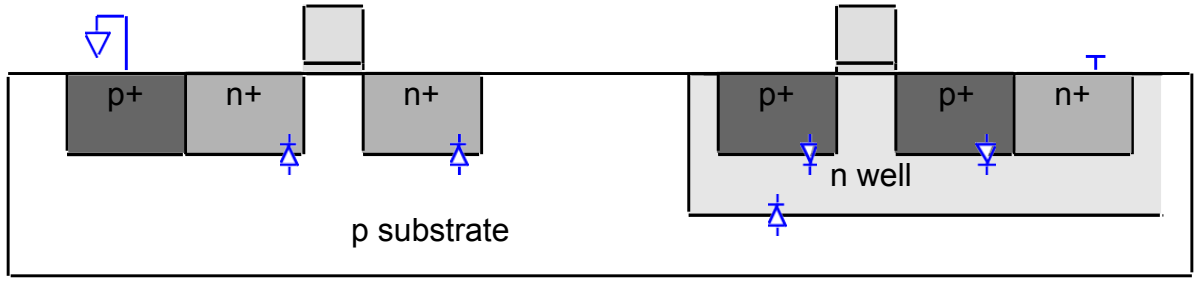
1) It becomes worse by drain induced barrier lowering in which a positive V_{ds}effectively reduces V_t. This effect is especially pronounced in short channel transistors.

Junction Leakage:

- The P-n junction between diffusion and the substrate or well form diodes are shownbelow.
- The substrate and well are tied to GND or V_{DD} to ensure that these diodes remain reversebiased.
- The reverse biased diodes still conduct a small amount of current Io.

$$I_D = I_s [e \frac{V_D}{V_T} - 1]$$

Wher
e I_D = diode current
I_s = diode reverse- biased saturation current that depends ondopinglevels andon the area and perimeter of the diffusion region.



Tunneling :

Based on quantum mechanics, we see that the is a finite probability that carriers will tunnel through the gate oxide. This results in gate leakage current flowing into the gate.
The probability of tunnelling drops off exponentially with oxide thickness.

- Large tunnelling currents impact not only dynamic nodes but also quiescent power consumption and thus may limit oxide thicknesstor.
- Tunnelling can purposely be used to create electrically erasable memory devices. Different dielectrics may have different tunnetingproperties.

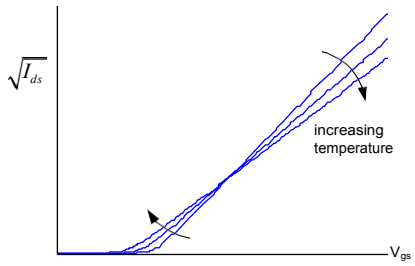
Temperature Dependance:

Temperature influences the characteristics of transistors. Carrier mobility decreases with temperature.

- Junction leakage increases with temperature because. I_s is strongly temperature dependent . The combined temperature effect is shown below.

Where on current decreases and OFF current increases with temperature.
The figure below shows how the On current I_{dsat} decreases with temperature. Circuit performance is worst at high temperature, called negative temperature coefficient.

- Circuit performance an be improved by cooling . Natural convection, fans with heat sink, water cooling thin flim refrigerators, and liquid nitrogen can be used ascooling.



Advantages of Operating at low temperature:

1) velocity saturation occurs at higher fields providing morecurrent.
2) For high mobility , power issaved.
3) Wider depletion region results in less junctioncapacitance.

Geometry Dependance:

- The layout designer draws transistors with width and length ^{W} drawn and L drawn. The actual gate dimensions may differ by factors X_w andX_L.
- The source and drain trends to diffuse later under the gate by L_{Di} producing a shorter effective between source anddrain.

$$Leff = L_{drawn} + X_L - 2L_P$$

$$Weff = W_{drawn} + X_W - 2w_D$$

Long transistors experience less channel length modulation. In a process blow 0.25 μm the effective length of the transistor depends on the orientation of the transistor.

3.Explain in detail about the ideal I-V characteristics of a nMOS and pMOS device (NOV/DEC 2013)(MAY/JUN 2013)(NOV/DEC2014)

MOS transistors have three regions of operation:

_ Cutoff or subthreshold region

_ Linear region

_ Saturation region

The current and voltage (I-V) for an nMOS transistor in each of these regions. The model assumes that the channel length is long enough that the lateral electric field (the field between source and drain) is relatively low, which is no longer the case in nanometer devices.

This model is variously known as the *long-channel*, *ideal*, *first-order,* or *Shockley* model. Subsequent sections will refine the model to reflect high fields, leakage, and other nonidealities. The long-channel model assumes that the current through an OFF transistor is 0.

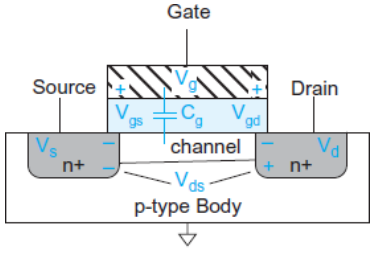
When a transistor turns ON (*Vgs*>*Vt*), the gate attracts carriers (electrons) to form a channel. The electrons drift from source to drain at a rate proportional to the electric field between these regions.

We know that the charge on each plate of a capacitor is *Q* = *CV*. Thus, the charge in the channel *Q*channel is

$$Q_{channel}=C_g(V_{gs}-V_t)$$

where *Cg* is the capacitance of the gate to the channel and *Vgc- Vt* is the amount of voltage attracting charge to the channel beyond the minimum required to invert from p to n.

The gate voltage is referenced to the channel, which is not grounded. If the source is at *Vs* and the drain is at *Vd*, the average is *Vc*= (*Vs* + *Vd*)/2 = *Vs* + *Vds*/2. Therefore, the mean difference between the gate and channel potentials *Vgc*is *Vg* – *Vc*= *Vgs*– *Vds*/2, as shown inFigure.



Average gate to channel potential:

$V_{gc} = (V_{gs} + V_{gd})/2 = V_{gs} - V_{ds}/2$

We can model the gate as a parallel plate capacitor with capacitance proportional to area over thickness. If the gate has length *L* and width *W* and the oxide thickness is *t*ox, as shown in below Figure, the capacitance is

$$C_g=\varepsilon ox(WL/t_{ox})=CoxWL$$

where εox is the permittivity of free space, 8.85 × 10–14 F/cm, and the permittivity of SiO2 is *k*ox = 3.9 times as great. Often, the ox/*t*ox term is called *C*ox, the capacitance per unit area of the gateoxide.

Each carrier in the channel is accelerated to an average velocity, *v*, proportional to the lateral electric field, i.e., the field between source and drain. The constant of proportionality μ is called the*mobility*.

$$v = \mu E$$

The time required for carriers to cross the channel is the channel length divided by the carrier velocity: *L*/*v*. Therefore, the current between source and drain is the total amount of charge in the channel divided by the time required to cross

$$\begin{aligned} I_{ds} &= \frac{Q_{\text{channel}}}{L/v} \\ &= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \\ &= \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} \end{aligned}$$

$$\beta = \mu C_{\text{ox}} \frac{W}{L};\ V_{GT} = V_{gs} - V_t$$

The term *Vgs*– *Vt* arises so often that it is convenient to abbreviate it as *VGT* .

$$K' = \mu Cox$$

If *Vds*>*V*dsat*VGT*, the channel is no longer inverted in the vicinity of the drain; we say it is pinched off. Beyond this point, called the *drain saturation voltage*, increasing the drain voltage has no further effect on current. Substituting *Vds*= *V*dsat at this point of maximum current in above eqn, we find an expression for the saturation current that is independent of*Vds*.

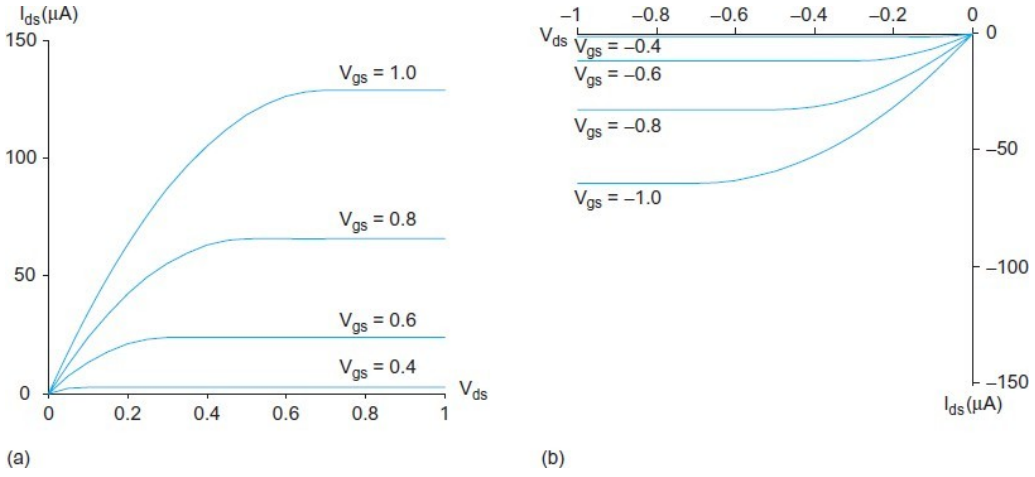
$$Ids=(\beta/2)V^2_{GT}$$

This expression is valid for *Vgs*>*Vt* and *Vds*>*V*dsat . Thus, long-channel MOS transistors are said to exhibit *square-law behavior* in saturation. Two key figures of merit for a transistor are *I*on and *I*off. *I*on (also called *I*dsat) is the ON current, *Ids*, when *Vgs*= *Vds*= *VDD*. *I*off is the OFF current when *Vgs*= 0 and *Vds*= *VDD*. According to the long-channel model, *I*off = 0 and

$$I_{on}=(\beta/2)(V_{dd}-V_t)$$

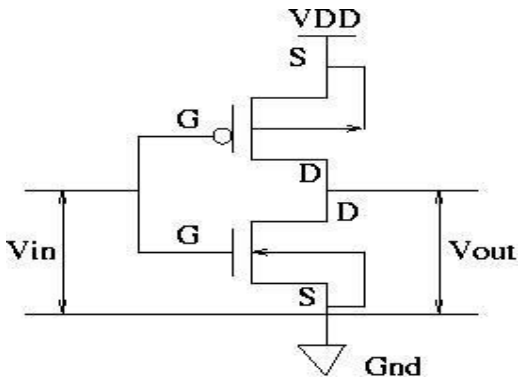
$$I_{ds}=\begin{cases} o & ; V_{gs} <- V_t \text{ ; cutoff} \\ (V_{gs}- V_t - V_{ds}/2)V_{ds} & ; V_{ds} < V_{dsat} \text{;linear} \\ \frac{\beta}{2}(V_{gs}- V_t)^2 & ; V_{ds} > V_{dsat} \text{ ;saturation.} \end{cases}$$

Below fig shows the I-V characteristics for the transistor. According to the first-order model, the current is zero for gate voltages below *Vt*. For higher gate voltages, current increases linearly with *Vds*for small *Vds*. As *Vds*reaches the saturation point *V*dsat = *VGT*, current rolls off and eventually becomes independent of *Vds*when the transistor is saturated. We will later see that the Shockley model overestimates current at high voltage because it does not account for mobility degradation and velocity saturation caused by the high electricfields.

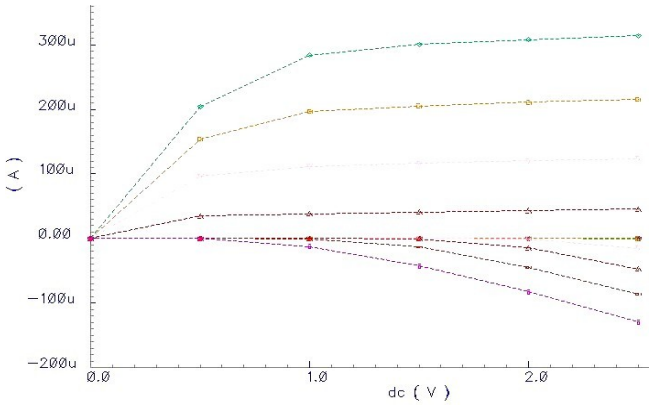


4.Explain in detail about DC characteristics of MoS transistor. (MAY/JUN2016/2022)

- A complementary CMOS inverter consists of a p-type and an n-type device connected inseries.
- The DC transfer characteristics of the inverter are a function of the output voltage (V_{out}) with respect to the input voltage (V_{in}).



- The MOS device first order Shockley equations describing the transistors in cut-off, linear and saturation modes can be used to generate the transfer characteristics of a CMOS inverter.
- Plotting these equations for both the n- and p-type devices produces the traces below.



- The DC transfer characteristic curve is determined by plotting the common points of V_{gs}intersectionaftertakingtheabsolutevalueofthep-deviceIVcurves,reflecting

them about the x-axis and superimposing them on the n-device IV curves.

- We basically solve for $V_{in(n\text{-}type)} = V_{in(p\text{-}type)}$ and $I_{ds(n\text{-}type)} = I_{ds(p\text{-}type)}$
- The desired switching point must be designed to be 50 % of magnitude of the supply voltage i.e. $V_{DD}/2$.
- Analysis of the superimposed n-type and p-type IV curves results in five regions in which the inverter operates.

- **Region A** occurs when $0 < V_{in} < V_{t(n\text{-}type)}$.
  - The n-device is in cut-off ($I_{dsn=0}$).
  - p-device is in linear region,
  - $I_{dsn} = 0$ therefore $-I_{dsp} = 0$
  - $V_{dsp} = V_{out} - V_{DD}$, but $V_{dsp} = 0$ leading to an output of $V_{out} = V_{DD}$.
- **Region B** occurs when the condition $V_{tn} < V_{in} < V_{DD}/2$ is met.
  - Here p-device is in its non-saturated region Vdsneq0.
  - n-device is in saturation

Saturation current Idsn is obtained by setting $V_{gs} = V_{in}$ resulting in the equation:

$$I_{dsn} = \frac{\beta_n}{2}\left[V_{un} - V_{tn}\right]^2$$

- In **region B** I_{dsp} is governed by voltages V_{gs} and V_{ds} described by:

$$V_{gs} = (V_{in} - V_{DD}) \text{ and } V_{ds} = (V_{out} - V_{DD})$$

$$I_{dsp} = -\beta_p\left[(V_{DD} - V_{DD} - V_{tn})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}\right]$$

- **Region C** has that both n- and p-devices are in saturation.

- **Region D** is defined by theinequality

$$\frac{V_{DD}}{2} < V_{in} \le V_{DD} + V_{tp}$$

- p-device is in saturation while n-device is in its non-saturationregion.

$$I_{dsp} = -\frac{\beta_p}{2}(V_{in} - V_{DD} - V)^2; V_{in} < V_{tp} + V_{DD}$$

AND

$$I_{dsn} = \beta_n \left| V_{in} - V_{tn} V_{out} - \left| \left(\frac{V_{out}}{2} \right)^2 \right| \right|; V_{in} > V_{tn}$$

- Equating the drain currents allows us to solve for Vout. (See supplemental notes for algebraicmanipulations).

- In **Region E** the input conditionsatisfies:

$$V_{in} \ge V_{DD} - V_{tp}$$

- The p-type device is in cut-off: $I_{dsp}=0$
- The n-type device is in linear mode
- $V_{gsp} = V_{in} - V_{DD}$ and this is a more positive value compared to V_{tp}.
- $V_{out} = 0$

5.Explain in detail about thepropagation delay. Delay Estimations:-

In most designs, there exist many logic paths called critical paths. These paths are recognized by a timing analyzer or circuit simulator. Critical paths are affectedby the following fourlevels.

i. Architecturallevel
ii. Logiclevel
iii. Circuitlevel
iv. Layoutlevel

Propagation delay time (t_{pd}) or max time is the maximum time from the input crossing 50%to the output crossing 50%.The delay can be estimated by the following ways,

i. RC delaymodels
ii. Linear delaymodels
iii. Logicefforts
iv. Parasiticdelay

1. **RC delaymodels:**

The delay of logic gate is computed as the product of RC,where R is the effective driver resistance and C the load capacitance. Logic gates use minimum –length devices for least delay, area and power consumption. The delay of a logic gate depends on the transistor width in the gate and the capacitance of the load.

Effective Resistance andCapacitance:

An NMOS transistor with width of one unit has effective esistance R An PMOS transistorwithwidthofoneunithaseffectiveresistance2RCapacitanceconsistsofgate capacitance c_g and source/diffusion capacitance c_{diff} .in most processes c_g is equal to c_{diff} , c_g and c_{diff} are proportional to transistorwidth.

Diffusion capacitance layouteffects:

To reduce the diffusion capacitance in the layout, diffusion nodes are shared. Uncontacted nodes have less capacitance. Diffusion capacitance depends on the layout.

2. **Elmore delaymodel:**

Elmore delay model estimates the delay of an RC ladder .this is equal to thesum overeachnode in the ladder of the resistance between the node and supply multiplied by capacitanceonthe node.

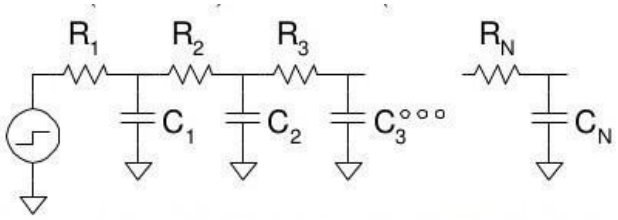


Fig: RC ladder for Elmore DelayModel

3. **Linear delaymodel:**

The propagation delay of a gate is d,

$$d = f + p$$

F= effort delay or state effort, which depends on the complexity and fan-out of the gate. P=parasitic delay

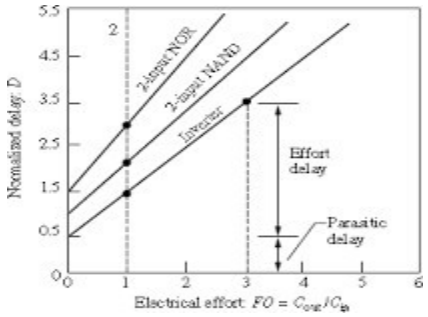


Fig: Normalized delay vs. fan-out

Logical effort:

Logical effort is defined as the ratio of the input capacitance of the gate to the input capacitance of an inverter that delivers the same output current.

Parasitic delay:

Parasitic delay is defined as the delay of the gate when it drives zero load. This can be estimated with RC delay models. The inverter has 3 units of diffusion capacitance on theoutput.

Gate type	Number of				
	1 input	2	3	4	n
INVERTER	1				
NAND		2	3	4	N
NOR		2	3	4	n
TRISTATE,MULTIPLEXER	2	4	6	8	2n

Logical effort and transistor sizing:

Logical effort provides a simple method to choose the best topology and number of stages of logic for a function. This quickly estimates the minimum possible delay for the given topology and to choose gate sizes that achieve thisdelay.

Delay in multistage logic networks:

Logical effort is independent of size and electrical effort is dependent onsize.

1. path logicaleffort
2. path electricaleffort
3. patheffort
4. branchingeffort
5. path branchingeffort
6. pathdelay
7. minimum possibledelay

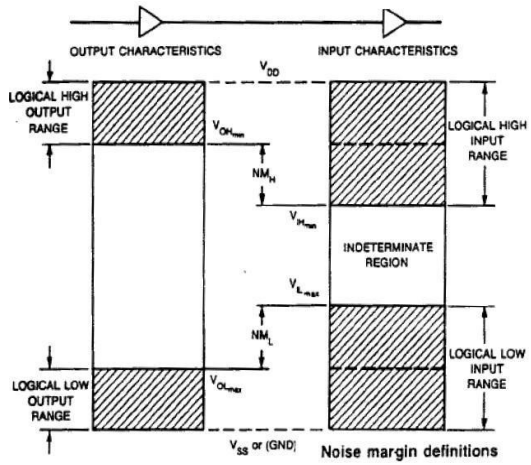
Choosing the best number ofstages:

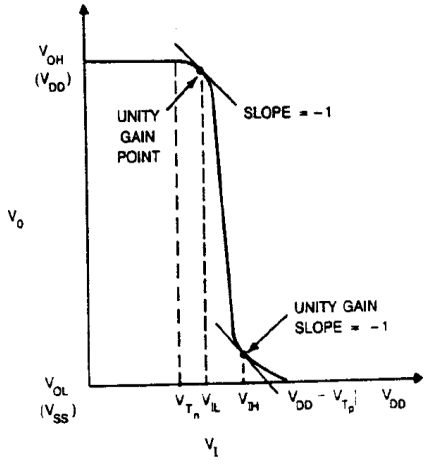
Inverters can be added at the end of a path without changing its function. Extra inverters and parasitic delay, but do not change the path logicaleffort.

***4.Derive the noise margins for CMOS inverter.*(Nov/Dec-16)**

DefinitionandT ypes:*(4Marks)*

NoiseMargin: Noisemarginisaparameterrelatedtoinputoutputcharacteristics.Itdetermines the allowable noise voltage on the input so that the output is not affected. We will specifyitin termsoftwothings:LOWnoisemarginHIGH noisemargin.





LOW noise margin: is defined as the difference in magnitude between the maximum Lowoutput voltage of the driving gate and the maximum input Low voltage recognized by the driven gate.

NML=|VILmax–VOLmax|

HIGH noise margin: is defined difference in magnitude between minimum High outputvoltageofthedrivinggateandminimuminputHighvoltagerecognizedbythereceivinggate.

NMH=|Vohmin–VIHmin

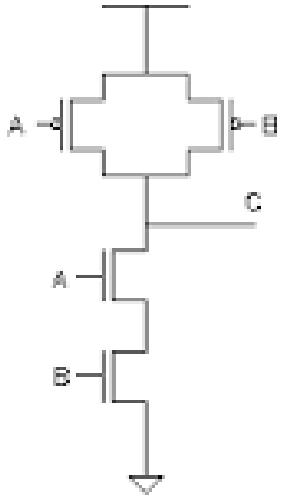
6.Write the layout design rules and Draw the layout diagram for NAND and NOR gate. (Nov/Dec-17,Apr/May-17)

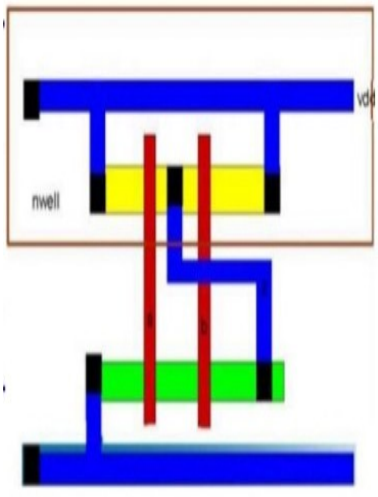
- **Design Rules:**

  Design rules represent a tolerance that ensures high probability of correct fabrication-rather than a hard boundary between correct and incorrect fabrication.

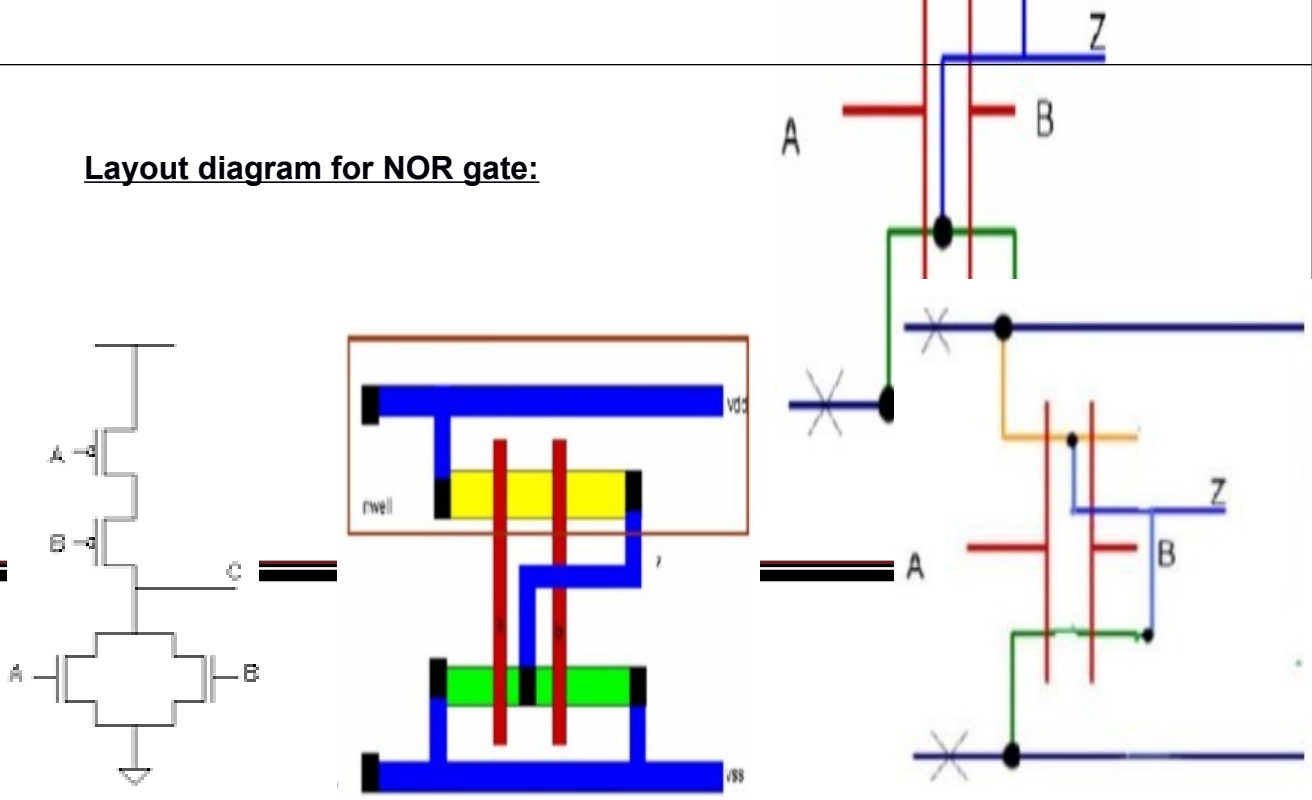
  - ✓ Micron design rule*(1Mark)*
  - ✓ Lambda design rule*(1Mark)*

Layout diagram for NAND gate:





Layout diagram for NOR gate:



6. Explain in detail about scaling concept. (MAY/JUN 2016)

(or)

Discuss on transistor and interconnect scaling

Scaling:

- As the transistors become smaller, they switch faster, dissipate less power and are cheaper to manufacture. Despite the ever increase is challenges process advances have actually accelerated in the pastdecade.
- Such scaling is unprecedented in the history of technology. However scaling also exacerbar noise and reliability issues and introduces newproblems.
- Designers need to be able to predict the effect of this feature size scaling on chip performance to plan future products, ensures existing products will scale gracefully to future processes for cost reduction and anticipate looming design challenges.

Transistor Scaling:

The characteristics of an MOS device can be maintained and the basic operational characteris. Can be preserved if the critical parameters of a device are scaled by a dimensionless factor . These parameters include.

º All dimensions (x,y, z directions)

º Device voltages

º Doping concentration densities.

Another approach is **lateral Scaling** , in which only the gate length is scaled. This is commonly called a gate shrink because it can done easily to an existing mask database for a design.

For **constant field scaling**, all devices dimension including channel length L, width W and oxide thickness t_{or} are reduced by a factor of 1/s. The supply voltage VDD and the threshold voltages are also reduced by1/s.

- The substrate doping WA is increasedby.
- Because both distance and voltage are scaled equally, the electric field remain constant.
- A gate shrink scales only the channel leng leaving other dimensions, voltages and doping levelsunchanged.
- This offers a quadratic improvement in gate delay according to the first order model.
- The gate delay improvement is closer to linear because velocity saturation keeps the current and effective resistance appronimatelyconstant.
- The constant voltage scaling increased the electric fields in the devices. By the 1 μ m generation velocity saturation was servere enough that decreasing feature size no longer improved devicecurrent.

Inter connect Scaling:

- Two common approaches to interconnect scaling are to either scale all dimensions or keep the wire heightconstant.
- Wire length decreases for some types of wires, but may increase for others? Local are scaled wires are those that decrease in length duringscaling.
- Example: A wire across 64 bits ALU is local because it becomes shorter as the ALU is migrated to finer process. A wire across a particular micro processer is scaled because when the microprocessor is shrunk to the new process the wire will alsoshrink.
- Un repeated interconnect delay is remaining about constant for local interconnect and increasing for global interconnect . This presents a problem because transistor are getting faster, So the ratio if interconnect to gate delay interconnect with scaling.
- In moders process with aspect ratios 1-5-22 fringing capacitance accounts for

the majority of the totalcapacitance.

- Scaling spacing but not height interconnect the fringing capacitance enough that the extra thickness scarcely improvesdelay.
- Observe that when wire thickness is called the capacitance per unit length remains constant. Hence, a reasonable initial estimate of the capacitance ofa minimum-pitch were is about 0.2fF/ μm, independent of the process.
- Wire capacitance is roughly 1/10-1/6 of gate capacitance per unitlength.

Impacts on Design:

- One of the limitations of first order scaling is that it gives the wrong impression of being able to scale proportionally to zero dimensions and zerovoltage.

Improved performance and cost:

- The most positive impact of scaling is that performance and cost are steadily improving. System architects need to understand the scaling of CMOS technologies and predict the capabilities of the process several years into the future, when a chip will becompleted.

Interconnect :

Scaling transistors are steadily improving in delay but scaled wires are holding constant or getting worse.

- The wire problem motivated a number of papers predicting the demise of conventionalwires.
- The plot is misleading in twoways.
- Firstthegatedelayisshownforasingleunloaded transistor rather than a realisticallyloadedgate.|Second,thewiredelayshownforfixedlengibutas μ technology scales, most local wires connecting gates within a unit also become shorter.

Power:

In classical constant field scaling, power density remains constant and overall chip power increases only slowly with die size.

- Power density has sky rocketed because clock frequencies have increased much faster to classical scaling would predict and V_{DD} is some what higher than constant field scaling woulddemand.
- Dynamic power consumption will not continue to increase at such rates

because it will become uneconomical to cool thechips.

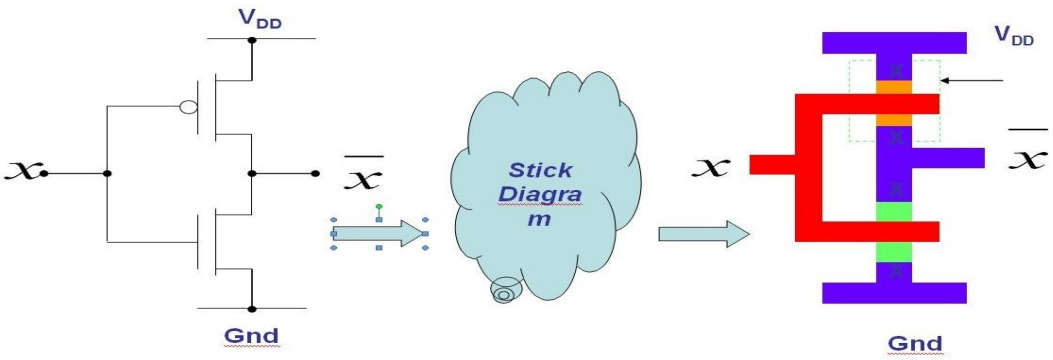
- The static power consumption caused by sub threshold leakage was historically negligible but becomes important for threshold voltage below about 0.3 to 04v.

7. Explain the stick diagram and layout diagram with examples. May 11,May13, Nov/Dec10

Stick diagrams:

Stick diagrams are used to convey layer information through the use of a colour code for example in NMOS design.

- Green for n-diffusion
- Red for polysilicon
- Blue formetal
- Yellow forimplant
- Black for contactareas
- The designer can draw a layout using coloured lines to represent the various process layers such as diffusion, metal and polysilicon.
- Where poly siliconcrossesthe diffusion, transistors are created and where metal wires join diffusion or poly silicon, contacts areformed.
- A stick diagram is a cartoon of a chip layout. They are not the exact models of layout.
- The stick diagram represents the rectangles with lines which represents wires are componentsymbols.
- The colour cooling has been complemented by monochrome encoding of the lies so the black and white copies of stick diagrams do not lose the layerinformation.
- The colour and monochrome encoding scheme used has been evolved to cover NMOS and CMOSprocesses.
- To illustrate the stick diagram inverter circuits are presented below in NMOS, and in P well CMOS technology.



- Having conveyed layer information and topology by using stick or symbolic diagrams. These diagrams relatively easily turned into masklayouts.
- The below diagram stressing the ready translation into mask layout form. In order that the mask layout produced during design will be compactible with the fabricationprocess.

  Aser of design rules are set out for layouts.

Stick diagram using NMOS Design:

We consider single metal, single poly silica NMOS technology. The layout of NMOS involves.

- N-diffusion and other thin oxide regions-green
- Polysilicon -red
- Metal -blue
- Impant -yellow
- Contacts - black orbrown

A transistor is formed wherever poly silicon crosses n-diffusion and all diffusion wires are n-type. The various steps involved in the design style are.

Step1: Draw the metal VDD and GND rails in parallel allowing enough space between them for the other circuit element which will be required.

Step 2: Draw the thinox paths between the rails for inverters and inverter based logic.

Step 3: Draw the pull up structure which comprises a depletion mode transistor interconnected between the output point and V_{DD}.

Step 4:

Draw the pull down structure comprising an enhancement mode structure interconnected between the output point and GNO.

Step 5: Signal paths may be switched by pass transistor, and along signal paths often require metal buses.

Design Rules and layout:

The design rules primarily address two issue

1) The geometrical reproduction of features that can be reproduced by the mask-making and lithographicalprocess.
2) The interactions between different layers. There are several approaches that can

be taken in describing the design rules. Theseinclude

- Micron designrules:
  - Stated at some micronresolution
  - Usually given as a list of minimum feature sizes and spacings for all masks required in a given process.
  - Normal style forindustry.
- Lambda (λ) based design rules
  - These rules popularized by Mead and Conway are based on a single parameter, λ which charactized the linear feature- the resolution of the complete wafer implementation process – and permits first orderscaling.
  - They have been widely used, particularly in the educational context and in the design of multi projectchips.

Layout (λ) based design Rules:

The lambda, λ design rules are bases on mead and Conway work and in gereral, design rules and layout methodology are based on the concept of λ which provides a process and feature size. Independent way of making mask dimensions to scale.

- Allpathsinalllayerswillbedimensionedinλunitsandsub-sequentlyλcan be allocated an appropriate value compactible with the feature size of the fabricalion process.
- Design rules can be conveniently set out in diagrammatic form as shown below.

Contact cuts:

The contacts between layers are set out as shown below. Here it will be obserred that connection can be made between two or, in the case of NMOs design, three layers.

1) Metal to poly silicon or todiffusion

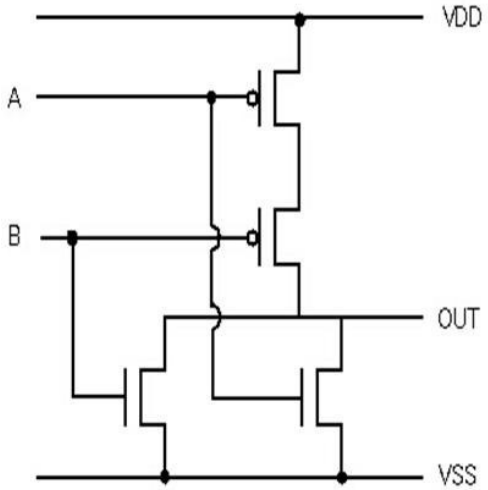
There are three possible approaches for making contacts between poly silicon and diffusion in NMOS circuits. Thereare

i) Poly silicon to metal then metal todiffusion

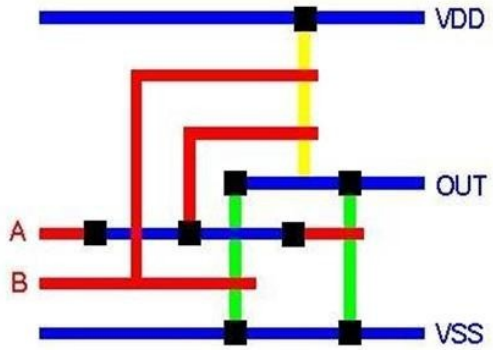
ii) Buried contact poly silicon to diffusion

iii) Buttingcontact.

- The 2 λ x2 λ contac cut indicates and area in which the oxide is to be removed down to the underlying polysilicon or diffusionsurface.
- When the deposition of the metal layer takes place, the metal is deposited through the contact cut areas on to the underlying areas so that contact is made between thelayers.



NOR gate in CMOS



UNIT II

COMBINATIONAL LOGIC CIRCUITS

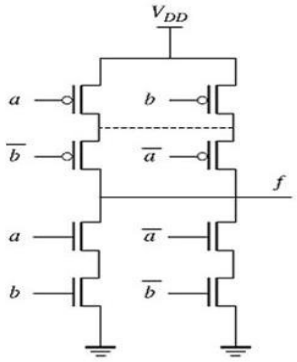
PART A

1. What is bubblepushing?

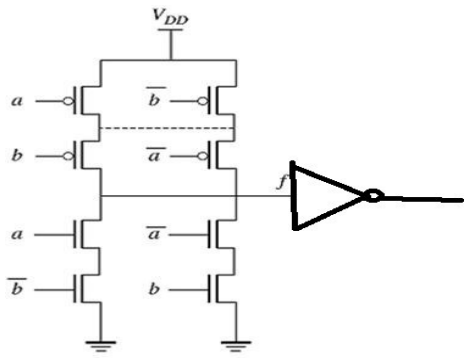
- CMoS gates are inherently inverting, so AND and OR functions must be built from NAND and NOR gates. Demorgans law helps with thisconversion.
- A NAND gate is equivalent to an OR of inverter inputs. A NOR gate is equivalent to an AND gate of inverter inputs. The same relationship applies to gates with more inputs switching between these representation is easy to do and is often called bubble pushing.

2. Draw XOR gate and XNOR gate using transmission gates.

XOR gate

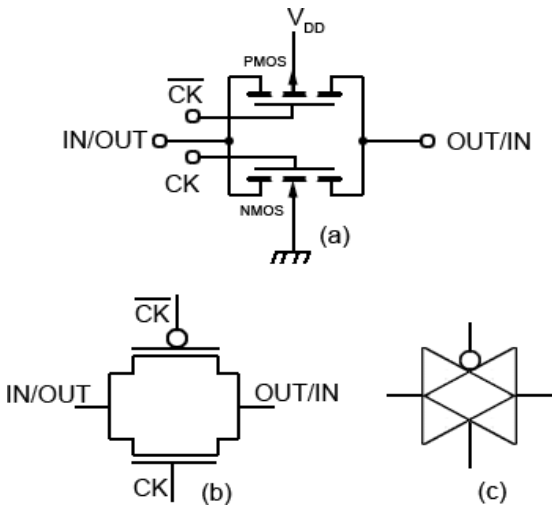


XNOR



3. **Write a note on CMOS transmission gate logic.(APRMAY2011)**

The transmission gate acts as voltage controlled resistor connecting the input and the output. It can be used as logic structure, switch, latch elementetc,.



4. **What are the factors that cause static power dissipation in CMOS circuits? (Nov/Dec2012)**

Static power dissipation due to:

- Sub threshold conduction through OFFtransistor.
- Tunneling current through gateoxide.
- Leakage through reverse biaseddiodes.

5. **List the various power losses in CMOS circuits. (Nov/Dec2013)**

Static power dissipation

Dynamic power dissipation

- Charging and discharging of loadcapacitance
- Short circuit curerent while both PMoS and nMoS networks arepartially ON

6. **State types of power dissipation .(APR/MAY2015)**

- Static powerdissipation
- Dynamic powerdissipation

7. **Define power dissipation.(NOV/DEC2013)**

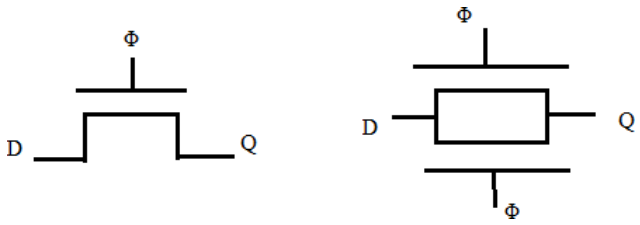
The instantaneous power p(t) drawn from the power supply is proportional to the supply current iDD(t) and the supply voltageVdd.

The energy consumed over sometime interval T is the integral of the instantaneous power.

8. **Implement a 2:1 multiplier using pass transistor(NOVDEC 2013)(APR/MAY 2015).**

When an nMoS or pMoS is used alone as an imperfect switch, it is called as apass transistor. By combining a nMoS and a pMoS transistor in parallel a switch is obtained that turns on when a 1 is applied to g in which 0's are passed in an acceptable fashion.this is a transmission gate or pass gate.

9. **Design a 1-bit dynamic register using pass transistor.(NOV/DEC2013)**



- The fig 1 shows a very simple transparent latch built from a single transistor it is compact and fast but suffers four limitations.
  - Fig 2 uses a CMoS transmission gate in place of the sinlgenMoS pass transistor to offer rail-rail output swings.

10. **Why single phase dynamic logic structure cannot be cascaded. justify(MAY/JUN 2016)**

In dynamic logic, a problem arises when caing one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which cannot be restored until the next clock cycle, so there is no recovery fromthis error

11. ***Whatarefactorsthatcausestaticpowerdissipationin CMOScircuits?*****(Nov/Dec-12)**

Powerdissipationduetoleakagecurrentwhentheidleiscalledthestaticpowerdissipation.

Staticpowerdueto

- Sub–thresholdconductionthroughOFFtransistors
- Tunnelingcurrentthroughgateoxide
- Leakagethroughreversebiaseddiodes
- Contention currentin radioed circuits.

13.Whatarethemethodstoreducedynamicpowerdissipation?

- Reducingtheproductofcapacitanceanditsswitchingfrequency.
- Eliminatelogicswitchingthatisnotnecessaryforcomputation.
- ReduceactivityfactorReducesupplyvoltage

14.Listvarious sourcesofleakagecurrents?

Various source of leakage currents are listened below:I1=Reverse-biasp-njunctiondiodeleakagecurrent.I2=band-to-band tunneling currentI3=Subthresholdleakagecurrent
I4=Gateoxidetunnelingcurrent
I5=GatecurrentduetohotcarrierjunctionI6=Channelpunchthrough
I7=Gateinduceddrainleakagecurrent

15.**List out the sources of static and dynamic power consumption. Or Define power dissipation.Statethetypesofpowerdissipation.*(Nov/Dec-17,Nov/Dec-16,Apr/may-15,Nov/Dec-13)***

- ***Static dissipation*** due to leakage current or other current drawn continuously from the power supply.
- ***Dynamic dissipation*** due to Switching transient current,Charging and discharging of load capacitances.

Types of Power dissipation:

There are three types of power dissipation.Theyare

- Static power dissipation.P_s=leakage power*supply voltage.
- Dynamic power dissipation.P_d==$C_L V^2_{dd} f_{clk}$
- Shortcircuitpowerdissipation.P_{sc}==I_{mean}*V_{dd}

17. Which MOS can pass logic1 and logic 0 stongly?

- p-mos can pass strong logic 1
- n-mos can pass strong logic 0

18. State the difference between Static CMOS and dynamic CMOS.

- Static CMOS circuits use or utilise complementary nMOS pulldown.
  - And pMOS pull-up networks to implement logic gates or logic functions in integrated circuits.
  - Dynamic gates use a clocked pMOS pullup.
- The enforced logic performs or the gate is achieved through 2 modes of operation: Precharge and choose.

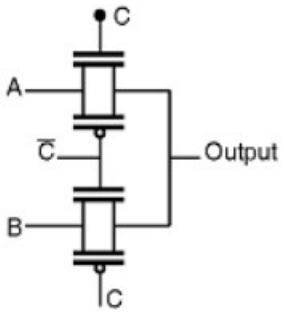
19. List the drawbacks of ratioed circuits.

- The drawbacks of ratioed circuits include slow rising transitions, contention on the falling transitions, static power dissipation, and a non-zero VOL.
- Dynamic Circuits: A dynamic logic gate uses clocking and charge storage properties of MOSFETs to implement logic operation.

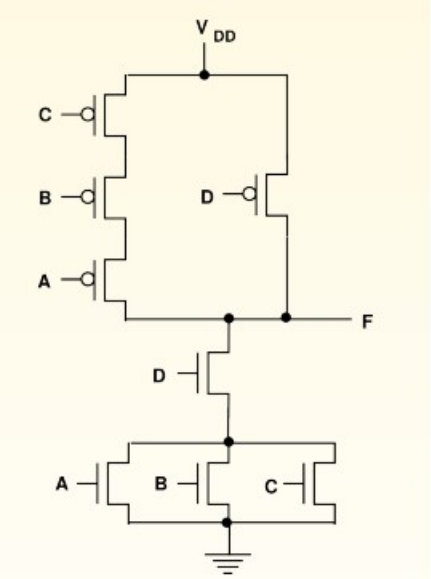
20. Define CVSL in CMOS.

Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. It requires mainly N-channel MOSFET transistors to implement the logic using true and complementary input signals, and also needs two P-channel transistors at the top to pull one of the outputs high. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).

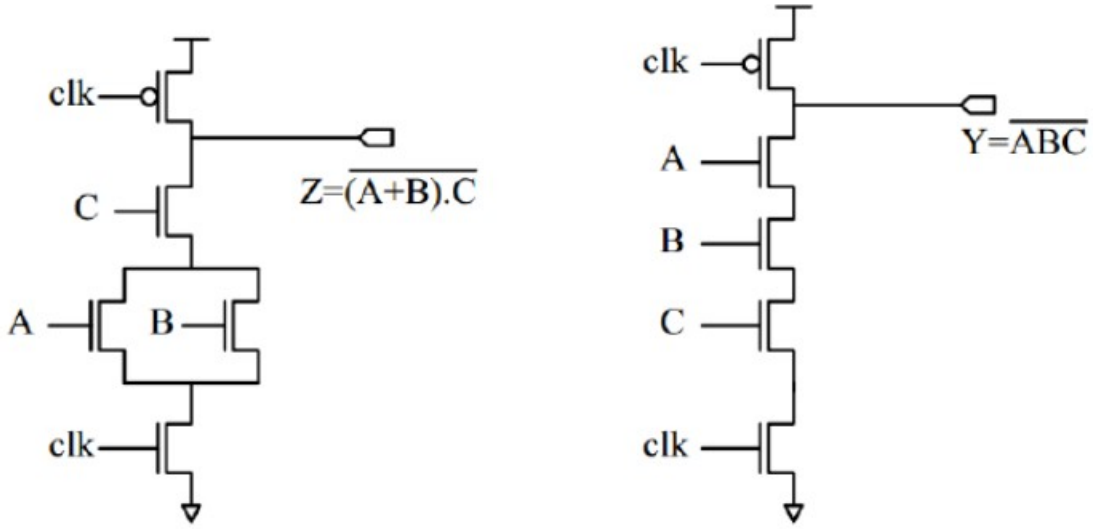
21. Draw the 2:1 mux using TG.



22.,Draw the static CMOS circuits ,F = (A + B + C) · D)

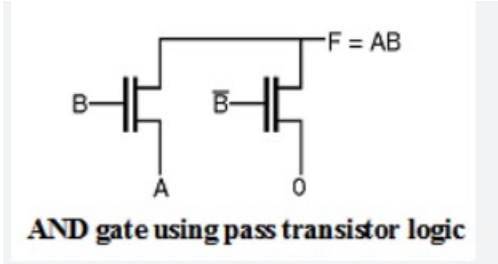


23. **Draw the dynamic CMOS circuits , Z= [(A + B) · C)]' and Y = (ABC)'.**



24. Define pass transistor logic with one example.

pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors.

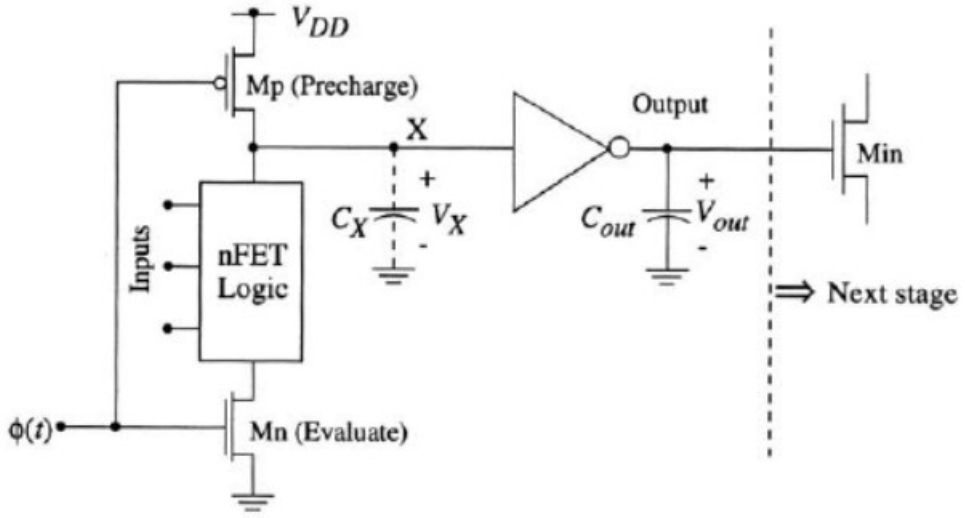


AND gate using pass transistor logic

.

25. State the function of domino logic in CMOS.

Domino logic is a system design style that eliminates the nMOS-nMOS glitch problem without introducing pMOS-type logic stages. The basis for domino circuits arises from once again studying the origin of the glitch problem in the nMOS-nMOS cascade.



PART-B

1. Write short notes on Static CMOS Design. (MAY'11,MAY'13)

The most widely used logic style is static complementary CMOS. The static CMOS style is really an extension of the static CMOS inverter to multiple inputs.

The primary advantage of the CMOS structure is robustness (i.e., low sensitivity to noise), good performance, and low power consumption with no static power dissipation. Most of those properties are carried over to large fan-in logic gates implemented using a similar circuit topology.

The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either VDD or Vss via a low-resistance path.

This is in contrast to the dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. The latter approach has the advantage that the resulting gate is simpler and faster. Its design and operation are however more involved and prone to failure due to an increased sensitivity to noise. The design of various static circuit flavors includes complementary CMOS, ratioed logic (pseudo-NMOS and DCVSL), and pass transistor logic.

a. ComplementaryCMOS

A static CMOS gate is a combination of two networks, called the pull-up network (PUN)and the pull-down network (PDN) (Figure 1). T

he figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs).

Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks are constructed in a mutually exclusive fashion such that one and only one of the networks is conducting in steady state.

In this way, once the transients have settled, a path always exists between VDD and

the output F, realizing a high output (“one”), or, alternatively, between VSS and F for a low output (“zero”). This is equivalent to stating that the output node is always alow-impedance node in steady

state.

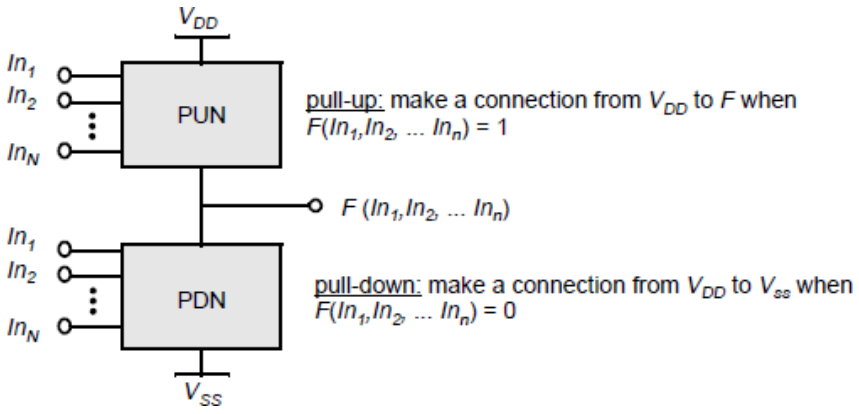


Figure 1: Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network).

In constructing the PDN and PUN networks, the following observations should bekept in mind:

- A transistor can be thought of as a switch controlled by its gate signal. An NMOS switch is on when the controlling signal is high and is off when the controlling signal is low. A PMOS transistor acts as an inverse switch that is on when the controlling signal is low and off when the controlling signal ishigh.
- The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce “strong zeros,” and PMOS devices generate “strong ones”. To illustrate this, consider the examples shown in Figure 2. In Figure 2.a, the output capacitance is initially charged to VDD.
- Two possible discharge scenarios are shown. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VTp| — the PMOS turns off at that point, and stops contributing discharge current.
- NMOS transistors are hence the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Figure 2.b, with the output initially at GND. A PMOS switch succeeds in charging the output all the way to VDD, while the NMOS device fails to raise the output above VDD-VTn. This

explains why PMOS transistors are preferentially used in a PUN.

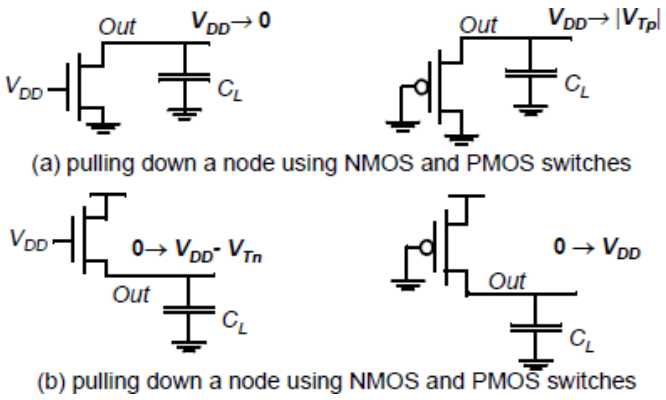


Figure 2 Simple examples illustrate why an NMOS should be used as a pull-down, and a PMOS should be used as a pull-up device.

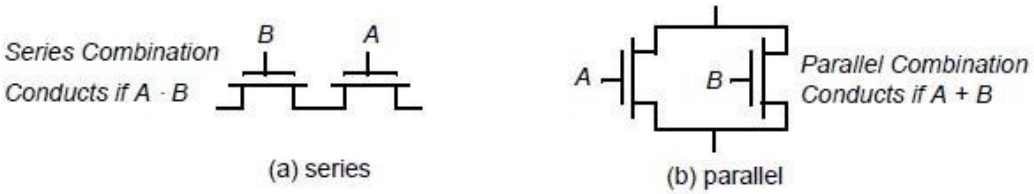


Figure 3 NMOS logic rules — series devices implement an AND, and parallel devices implement an OR.

A set of construction rules can be derived to construct logic functions (Figure 4). NMOS devices connected in series corresponds to an AND function. With all the inputs high, the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel represent an OR function. A conducting path exists between the output and input terminal if at least one of the inputs is high. Using similar arguments, construction rules for PMOS networks can be formulated. A series connection of PMOS conducts if both inputs are low, representing a NOR function (A.B = A+B), while PMOS transistors in parallel implement a NAND (A+B = A· B.

- The complementary gate is naturally inverting, implementing only functions such as NAND, NOR, and XNOR. The realization of a non-inverting Boolean function (such as AND OR, or XOR) in a single stage is not possible, and requires the addition of an extra inverterstage.
- The number of transistors required to implement an N-input logic gate is 2N.

b. II RatioedLogic

Ratioed logic is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation. The purpose of the PUN in complementary CMOS is to provide a conditional path between VDD and the output when the PDN is turned off. In ratioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output (Figure 5.a). Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull- down network that realizes the logic function, and a simple load device. Figure 5.b shows an example of ratioed logic, which uses a grounded PMOS load and is referred to as a pseudo- NMOSgate.

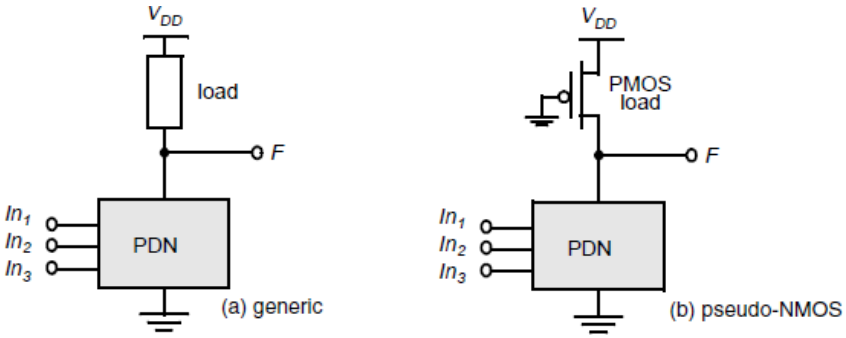


Figure 5: Ratioed logic gate.

The clear advantage of pseudo-NMOS is the reduced number of transistors (N+1versus 2N for complementary CMOS). The nominal high output voltage (VOH) for this gate is VDD since the pull-down devices are turned off when the output is pulled high (assuming that VOL is below VTn). On the other hand, the **nominal low output voltage is not 0 V** since there is a fight between the devices in the PDN and the grounded PMOS load device. This results in reduced noise margins and more importantly static power dissipation.

The sizing of the load device relative to the pull-down devices can be used to trade-off parameters such a noise margin, propagation delay and power dissipation. Since the voltage swing on the output and the overall functionality of the gate depends

upon the ratio between the NMOS and PMOS sizes, the circuit is called ratioed. This is in contrast to the ratioless logic styles, such as complementary CMOS, where the low and high levels do not depend upon transistorsizes.

Computing the dc-transfer characteristic of the pseudo-NMOS proceeds along paths similar to those used for its complementary CMOS counterpart. The value of VOL is obtained by equating the currents through the driver and load devices for Vin = VDD. At this operation point, it is reasonable to assume that the NMOS device resides in linear mode (since the output should ideally be close to 0V), while the PMOS load issaturated.

$$k_n\left((V_{DD}-V_{Tn})V_{OL}-\frac{V_{OL}^2}{2}\right) = k_p\left((-V_{DD}-V_{Tp})\cdot V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Assuming that VOL is small relative to the gate drive (VDD-VT) and that VTn is equal to VTp in magnitude, VOL can be approximatedas:

$$V_{OL}\approx\frac{k_p(-V_{DD}-V_{Tp})\cdot V_{DSAT}}{k_n(V_{DD}-V_{Tn})}\approx\frac{\mu_p\cdot W_p}{\mu_n\cdot W_n}\cdot\left|V_{DSAT}\right|$$

In order to make VOL as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. Unfortunately, this has a negative impact on the propagation delay for charging up the output node since the current provided by the PMOS device islimited.

A major disadvantage of the pseudo-NMOS gate is the static power that is dissipated when the output is low through the direct current path that exists between VDD and GND. The static power consumption in the low-output mode is easilyderived.

$$P_{low} = V_{DD}I_{low}\approx V_{DD}\cdot k_p\left((-V_{DD}-V_{Tp})\cdot V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)$$

2. Discuss in detail about the Dynamic CMOS design.(MAY'11)

Dynamic circuits overcome these drawbacks by using a clocked pull-up transistor rather than a pMOS that is always ON. Dynamic circuit operation is divided into two modes, as shown in Figure 9.22. During Precharge, the clock K is 0, so the clocked pMOS is ON and initializes the output Y high. During evaluation, the clock is 1 and the clocked pMOS turns OFF. The output may remain high or may be discharged low through the pull down network. Dynamic circuits require careful clocking, consume significant dynamic power, and are sensitive to noise duringevaluation.

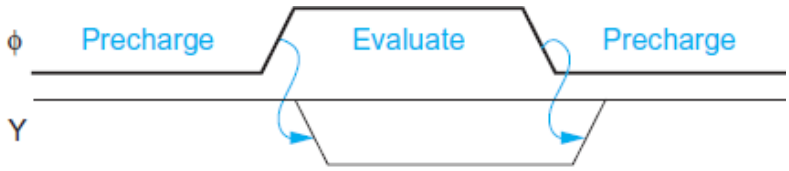


FIGURE 9.22 Precharge and evaluation of dynamic gates

If the input A is 1 during Precharge, contention will take place because both the pMOS and nMOS transistors will be ON. When the input cannot be guaranteed to be 0 during Precharge, an extra clocked evaluation transistor can be added to the bottom of the nMOS stack to avoid contention as shown in Figure 9.23. The extra transistor is sometimes called a foot. Figure 9.2 shows generic footed and unfooted gates.

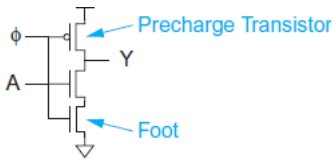


FIGURE 9.23 Footed dynamic inverter

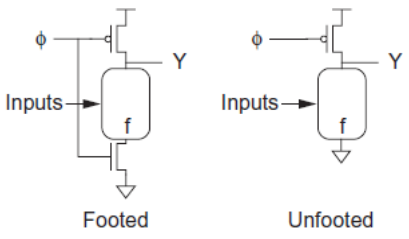


FIGURE 9.24 Generalized footed and unfooted dynamic gates

Figure 9.25 estimates the falling logical effort of both footed and unfooted dynamic gates. Footed gates have higher logical effort than their unfooted counterparts but are still an improvement over static logic.

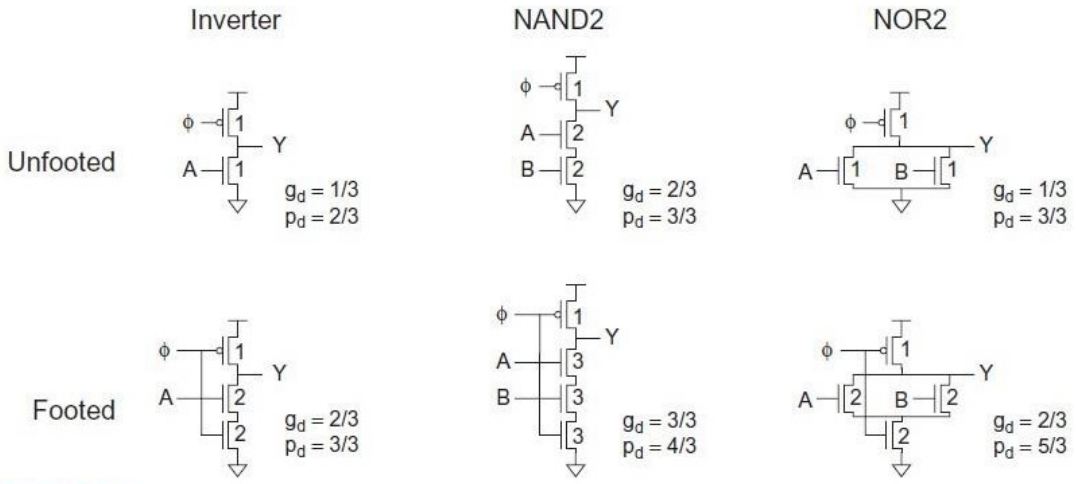


FIGURE 9.25 Catalog of dynamic gates

A fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. That is, the input can start LOW and remain LOW, start LOW and rise HIGH, start HIGH and remain HIGH, but not start HIGH and fall LOW.Figure

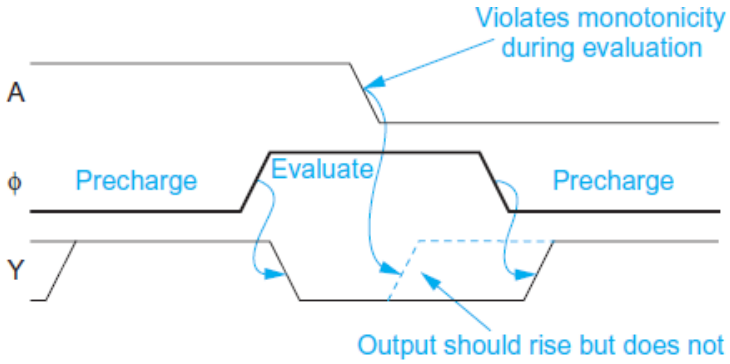


FIGURE 9.26 Monotonicity problem

shows waveforms for a footed dynamic inverter in which the input violates monotonicity.

The output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a seconddynamic

gate expecting monotonically rising signals, as shown in Figure 9.27. Dynamic gates sharing the same clock cannot be directlyconnected.

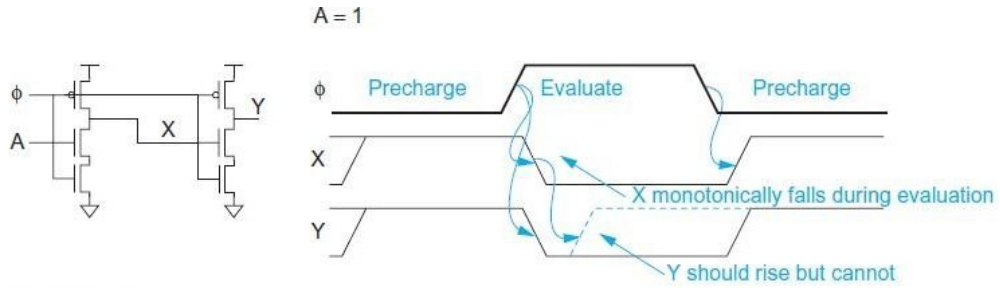


FIGURE 9.27 Incorrect connection of dynamic gates

Advantages

- Lower inputcapacitance
- No contention duringswitching
- Zero static powerdissipation

Disadvantages

- Require carefulclocking
- Consume significant dynamicpower
- Sensitive tonoise

Applications

- Used in wide NORfunctions
- Used inmultiplexers

The various drawbacks can be overcome by the followinglogics:

- Dominologic
- Dual-rail Dominologic
- Keepers
- Multiple output Dominologic
- NP and ZipperDomino

a. DominoLogic

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates, as shown in Figure 9.28(a). This converts the monotonically falling output into a monotonically rising signal suitable for the next gate, as shown in Figure 9.28(b). The dynamic-static pair together is called a domino gate because Precharge resembles setting up a chain of dominos and evaluation causes the gates to fire like dominos tipping over, each triggering the next. A single clock can be used to Precharge and evaluate all the logic gates within the chain. The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising. Therefore, the static inverter is usually a HI-skew gate to favor this rising output. Observe that Prechargeoccurs inparallel,but evaluation occurs sequentially. The symbols for the dynamic NAND, HI-skew inverter, and domino AND are shown in Figure9.28(c).

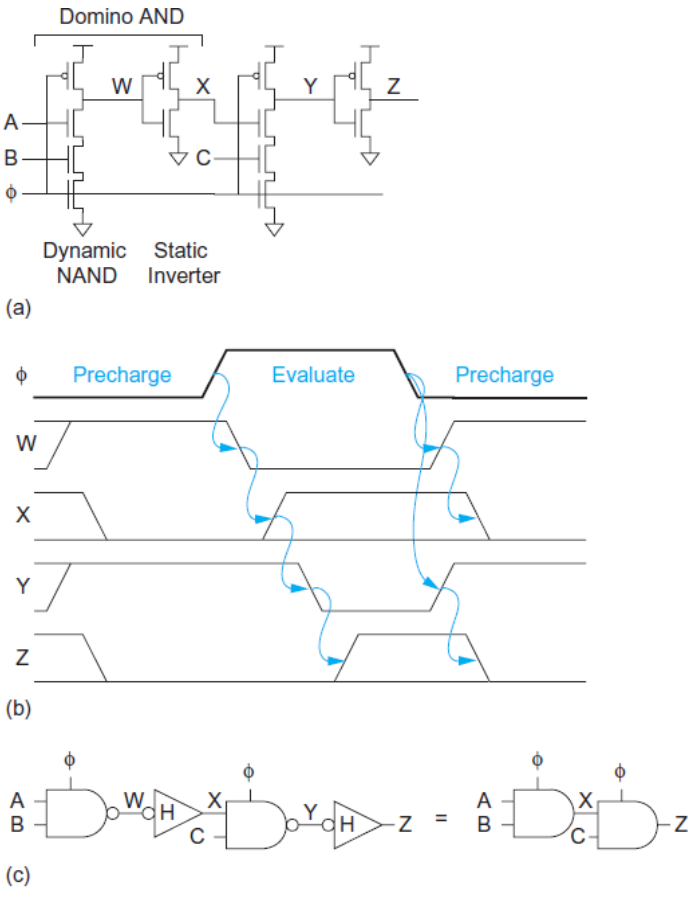


FIGURE 9.28 Domino gates

b. Dual-Rail Domino Logic

Dual-rail domino gates encode each signal with a pair of wires. The input and output signal pairs are denoted with _h and _l, respectively. The _h wire is asserted to indicate that the output of the gate is “high” or 1. The

_l wire is asserted to indicate that the output of the gate is “low” or 0. When the gate is Precharge, neither _h nor _l is asserted. The pair of lines should never be both asserted simultaneously during correct operation. Dual-rail domino gates accept both true and complementary inputs and compute both true and complementary outputs, as shown in Figure 9.30(a). Observe that this is identical to static CVSL circuits from Figure 9.20 except that the cross-coupled pMOS transistors are instead connected to the Precharge clock. Therefore, dual-rail domino can be viewed as a dynamic form of CVSL, sometimes called DCVS. Figure 9.30(b) shows a dual-rail AND/NAND gate and Figure 9.30(c) shows a dual-rail XOR/XNORgate.

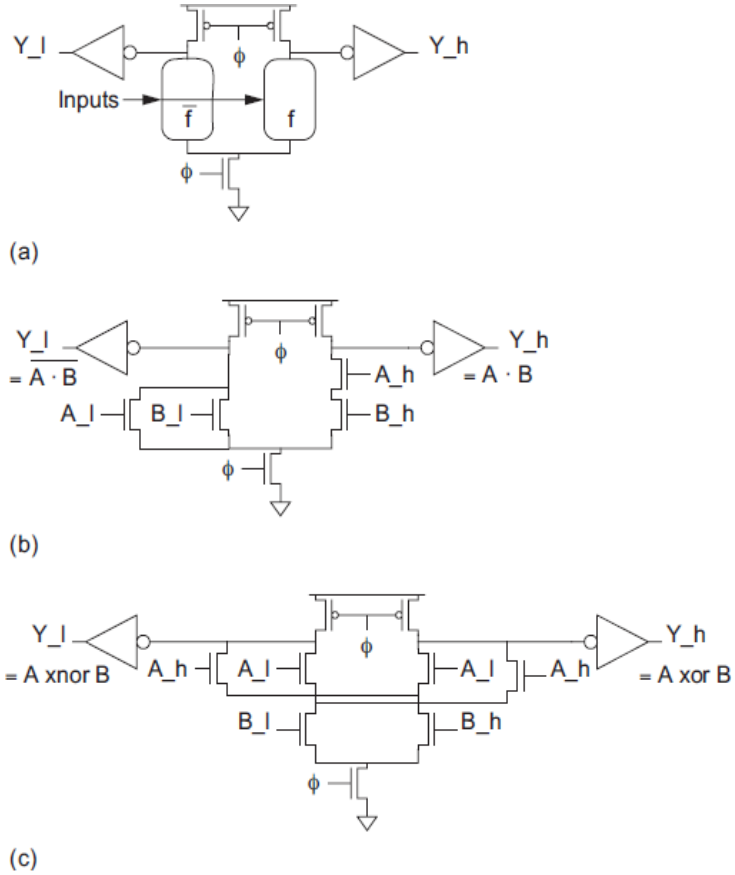


FIGURE 9.30 Dual-rail domino gates

Dual-rail structures also neither lose the efficiency of wide dynamic NOR gates because they require complementary tall dynamic NAND stacks. Dual-rail domino signals not only the result of a computation but also indicates when the computation is done. Before computation completes, both rails are Precharge. When the computation completes, one rail will be asserted. A NAND gate can be used for completion detection, as shown in Figure 9.31. Coupling can be reduced in dual-rail signal busses by inter digitating the bits of the bus, as shown in Figure 9.32. Each wire will never see more than one aggressor switching at a time because only one of the two rails switches in each cycle.

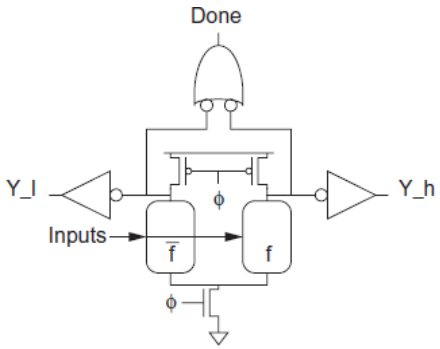


FIGURE 9.31 Dual-rail domino gate with completion detection

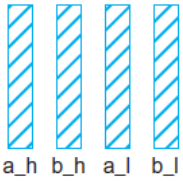


FIGURE 9.32 Reducing coupling noise on dual-rail busses

c. Keepers

Dynamic circuits also suffer from charge leakage on the dynamic node. If a dynamic node is precharged high and then left floating, the voltage on the dynamic node will drift over time due to sub threshold, gate, and junction leakage. The time constants tend to be in the millisecond to nanosecond range, depending on process and temperature. This problem is analogous to leakage in dynamic RAMs. Moreover, dynamic circuits have poor input noise margins. If the input rises above Vt while the gate is in evaluation,theinputtransistorswillturnonweaklyandcanincorrectlydischargethe

output. Both leakage and noise margin problems can be addressed by adding a keeper circuit. Figure 9.33 shows a conventional keeper on a domino buffer. The keeper is a weak transistor that holds, or staticizes, the output at the correct level when it would otherwise float. When the dynamic node X is high, the output Y is low and the keeper is ON to pre- vent X from floating. When X falls, the keeper initially opposes the transition so it must be much weaker than the pull down network. Eventually Y rises, turning the keeper OFF and avoiding static powerdissipation.

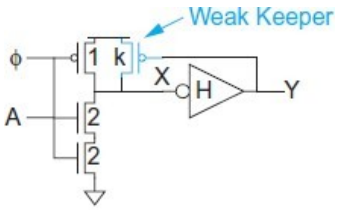


FIGURE 9.33 Conventional keeper

d. Multiple-Output Domino Logic(MODL)

It is often necessary to compute multiple functions where one is a subfunction of another or shares a subfunction. Multiple-output domino logic (MODL) [Hwang89, Wang97] saves area by combining all of the computations into a multiple-output gate. A popular application is in addition, where the carry-out $c_i$of each bit of a 4-bit block must be computed, as discussed in Section 11.2.2.2. Each bit position i in the block can either propagate the carry (p_i) or generate a carry (g_i). The carry-out logicis

$$c_1 = g_1 + p_1 c_0$$
$$c_2 = g_2 + p_2(g_1 + p_1 c_0)$$
$$c_3 = g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0))$$
$$c_4 = g_4 + p_4(g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0)))$$

This can be implemented in four compound AOI gates, as shown in Figure

9.44(a). Notice that each output is a function of the less significant outputs. The more compact MODL design shown in Figure 9.44(b) is often called a Manchester carry chain.

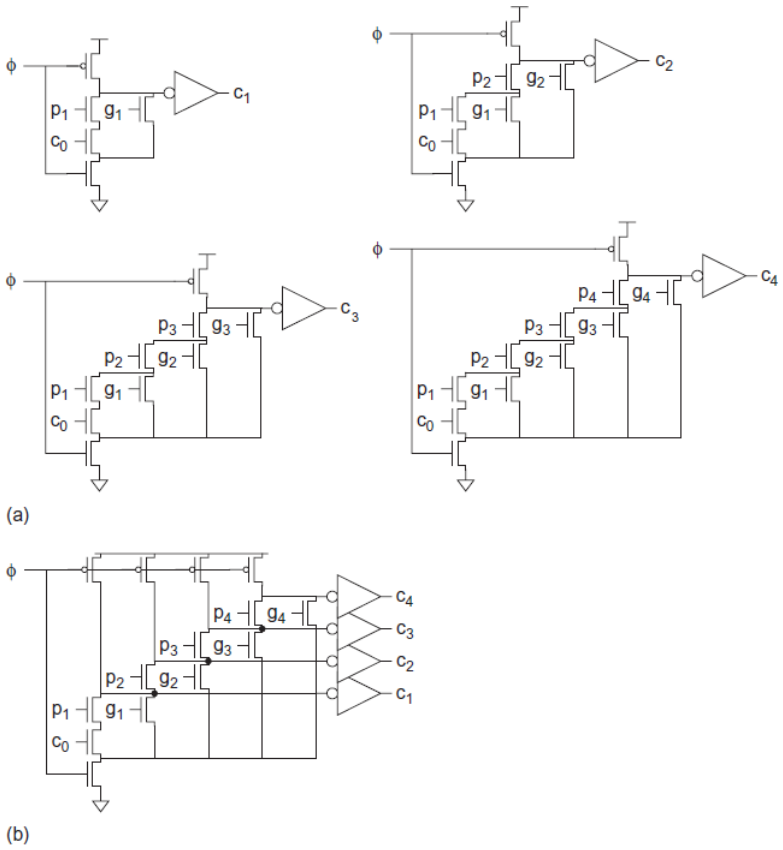


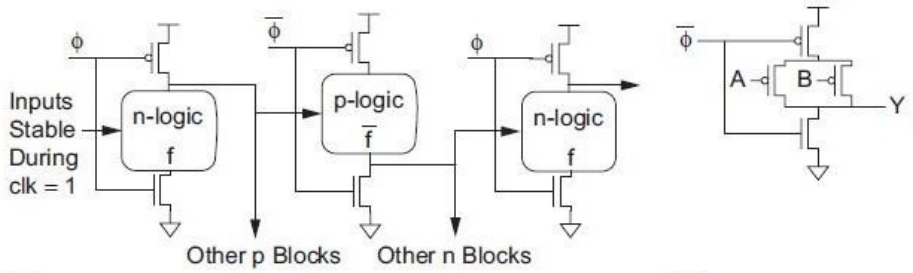
FIGURE 9.44 Conventional and MODL carry chains

e. NP and ZipperDomino

Another variation on domino is shown in Figure 9.46(a). The HI-skew inverting static gates are replaced with predischarged dynamic gates using pMOS logic. For example, a footed dynamic p-logic NAND gate is shown in Figure 9.46(b). When K is 0, the first and third stages precharge high while the second stage pre- discharges low. When K rises, all the stages evaluate. Domino connections are possible, as shown in Figure 9.46(c). The design style is called NP Domino or NORADomino.

Disadvantages

- Logical effort is theworst
- Susceptible tonoise



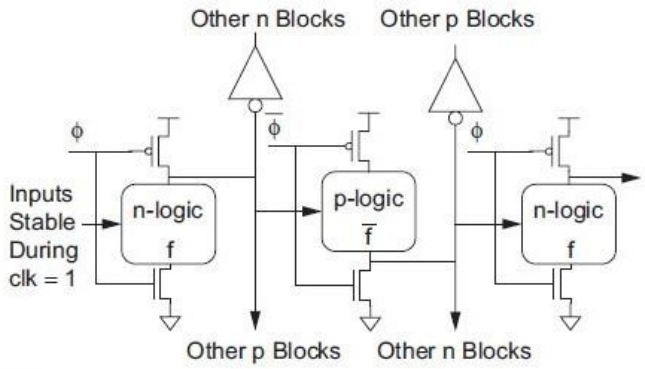


FIGURE 9.46 NP Domino

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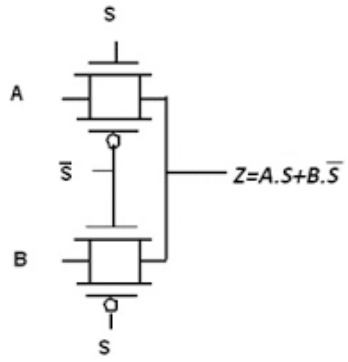
3. **a. Write a brief note on pass Transistor circuits also explain about CMOS with Transmission gates. (may 2011,2013) (MAY/JUN2016)**

Pass Transistor Circuits:

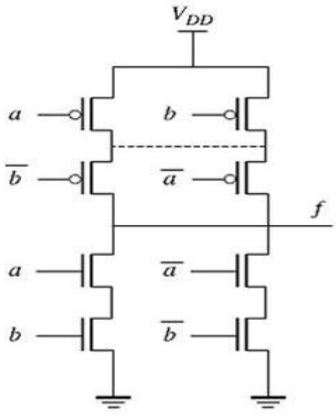
- In pass transistor circuits, inputs are also applied to the source/drain diffusion terminals.
- These circuits build switches using either n MOS pass transistor or parallel pairs of nM\OS and p MOS transistors called transmissiongates.
- For example pass transistors are essential to the design of efficient 6 transistor static RAM cells used in most modernsystems.
- Full address and other circuits rich in XOR s also can b efficiently constructed with passtransistors.

CMOS with Transmission Gates:

- Structures such as tristates, latches and multiplexers are often drawn as transmission gates in conjection with simple static CMOSLogic.
- The logic levels on the output are no better than those on the input so a cae of such circuits may accumulateNoise.
- To buffer the output and restore levels a static CMOS output inverter can be added.
- At first CMOS with transmission gates might appear to offer an entirely new range of circuits. The examination shows that the topology is almost identical to static CMOS.
- If multiple stages of logic are cae they can be viewed as alternating transmission gates aninverters.



- The above figure redrawsthemultiplexes to include the inverters from theprevious that drive the diffusion input but to exclude in outputinverter.
- The intermediate modes in the pull up and pull-down networks are shorted together as N_1 andN_2.



- The shorting of the intermediate nodes has two effects ondelay.
- Since the output is pulled up or down through the parallel combination of both pass transistor rather than through a single transistor. The effective resistance willdecreased.
- But the effective capacitance increases slightly because of extra diffusion and wire capacitance required for thisshorting.
- There are several factors that favour the static CMOS representation over CMOS with transmission gates.
- It the inverter is on the output rather than the input, the delay of the gate depends on what is driving the input as well as the capacitance drivar by the output.
- The second drawback is that diffuse inputs to tristate invertors are susceptible to noise that may incorrectly turn on theinverter.
- Finally the contacts slightly increases are and their capacitance increases powerconsumption.
- The logical effort of circuits involving transmission gates is computed by drawing stage that begin at gate inputs rather than diffusioninputs.

Complementary pass Transistor Logic(CPL):

- CVSI is slow because one side of the gate pulls down, and then the cross coupled PMOs transistor pulls the other sideup.
- The size of the cross coupled device is an inherent compromise between a large transistor that fights the pull down excessively and a small transistor that is slow pullingup.
- CPL resolves this problem by making on half of the gate pull up while the other half pullsdown.
- In theCPLmultiplexer. If a path consists of a cae of CPL gates, the inverters can be viewed equally well as being on the output of one stage or the input of the neststage.
- If we redraws the mux to include the inverters from the previous stage that drives the diffusion input, but to exclude the outputinverters.
- When the gate switches, one side pulls down well through its n MOS transistor.

- The other side pullsup.
- CPL can be constructed without cross coupled PMOS transistors, but the outputs would only toV_{DD}-V_t.
- Adding weak cross- coupled devices helps bring the rising output to the supply rail while only slightly slowing the fallingoutput.

4. Explain about Pass-Transistor Logic.(MAY'13)

The implementation of the AND function constructed that way, using only NMOS transistors is shown in Figure 6.33. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by B seems to be redundant at first glance. Its presence is essential to ensure that the gate is static; this is that a low-impedance path exists to the supply rails under all circumstances, or, in this particular case, when B is low.

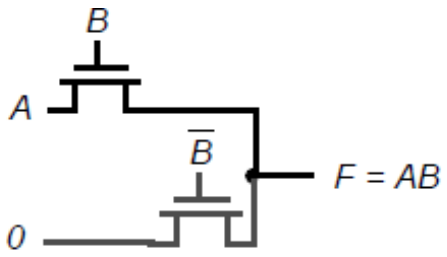


Figure 6.33 Pass-transistor implementation of an AND gate.

Differential Pass Transistor Logic

For high performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. These gates possess a number of interestingproperties:

- XOR's and adders can be realized efficiently with small number of transistors.
- CPL belongs to the class of staticgates
- Modulardesign

- All gates use sametopology

Advantages

- Conceptuallysimple
- Modular logicstyle
- Applicability depends on logicfunction
- Easy to realize adders andmultipliers

Disadvantages

- Has routingoverhead
- Suffers static powerdissipation
- Reduced noisemargin

Efficient Pass-Transistor Design

Differential pass-transistor logic, like single-ended pass-transistor logic, suffers from static power dissipation and reduced noise margins, since the high input to the signal-restoring inverter only charges up to VDD-VTn. There are several solutions proposed to deal with this problem as outlinedbelow.

Solution 1: Level Restoration: A common solution to the voltage drop problem is the use of a level restorer, which is a single PMOS configured in a feedback path (Figure 6.39). The gate of the PMOS device is connected to the output of the inverter, its drain connected to the input of the inverterand

the source to VDD. Assume that node X is at 0V (out is at VDD and the M_r is turned off) with B = VDD and A = 0. If input A makes a 0 to VDD transition, M_n only charges up node X to VDD-VTn. This is, however, enough to switch the output of the inverter low, turning on the feedback device M_r and pulling node X all the way to VDD. This eliminates any static power dissipation in the inverter. Furthermore, no static current path can exist through the level restorer and the pass-transistor, since the restorer is only active when A is high. In summary, this circuit has the advantage that all voltage levels are either at GND or VDD, and no static power isconsumed.

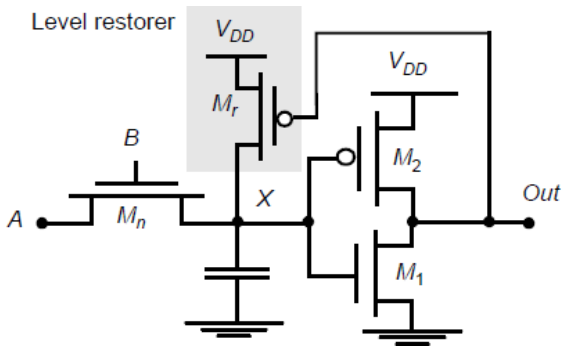


Figure 6.39 Level-restoring circuit.

Solution 2: Multiple-Threshold Transistors: A technology solution to the voltage-drop problem associated with pass-transistor logic is the use of multiple-threshold devices. Using zero threshold devices for the NMOS pass-transistors eliminates most of the threshold drop, and passes a signal close to VDD. Notice that even if the devices threshold was implanted to be exactly equal to zero, the body effect of the device prevents a swing to VDD. All devices other than the pass transistors (i.e., the inverters) are implemented using standard high-thresholddevices.

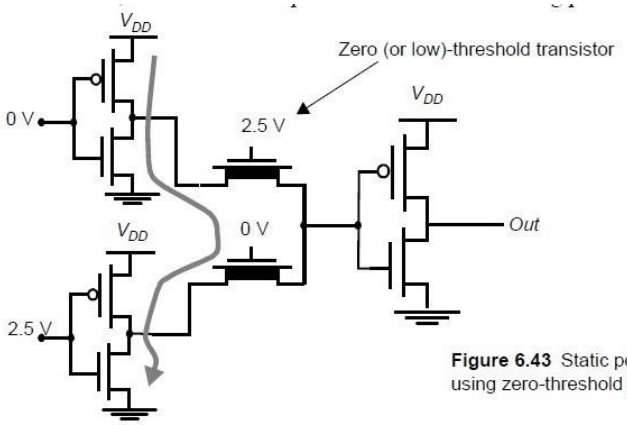


Figure 6.43 Static power consumption when using zero-threshold pass-transistors.

Solution 3: Transmission Gate Logic: The most widely-used solution to deal with the voltage- drop problem is the use of transmission gates. It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up. This gate either selects input A or B based on the value of the control signal S, which is equivalent to implementing the following Booleanfunction:

$$\overline{F} = (A \cdot S + B \cdot \overline{S})$$

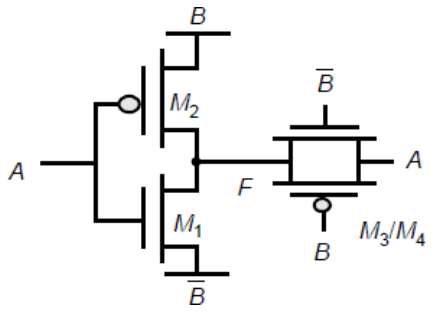


Figure 6.47 Transmission gate XOR.

A complementary implementation of the gate requires eight transistorsinsteadof six.

5. Explain the power dissipation present in VLSI circuits(APR/MAY 2010)(MAYJUN 2014)(APR/MAY 2015) (MAY/JUN 2016)

Or

5.Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions. Also explain how it can be reduced. ***(Apr/May-17, May/Jun-16, Nov/Dec-16,Apr/May-15,Nov/Dec-15, May/Jun-14,Nov/Dec-13)***

- **Static power dissipation:**

  - ✓ Duetoleakagecurrentorothercurrentdrawncontinuouslyfromthepowersupply.

Duetoleakagecurrentorothercurrentdrawncontinuouslyfromthepowersupply.

- ✓ Sub–thresholdconductionthroughOFFtransistors
- ✓ Tunnelingcurrentthroughgateoxide
- ✓ Leakagethroughreversebiaseddiodes
- ✓ Contention currentin radioed circuits.

$$P_{static}=(I_{sub}+I_{gate}+I_{junct}+I_{contention})V_{DD}$$

Staticpowerdissipation.P_s=leakagepower*supplyvoltage.

Reductionmethod: ***(3Marks)***

- ✓ One way to reduce power at the technological levelis to reduce the supply voltage.
- ✓ Thealternative approach to reducing waste ful activity

sapplyinganasynchronousdesign methodology.

- **Dynamicpowerdissipation:*(8Marks)***

Definition:

- ✓ Due to switching transient current,Charging and discharging of load capacitances.

Explanation:

Dynamic power:$P_{dynamic}=P_{switching}+P_{shortcircuit}$

- ✓ Switching load capacitances
- ✓ Short-circuit current-Both pMOS and nMOS stacks are partially ON
- ✓ Dynamic power dissipation.$P_d==C_LV^2_{dd}f_{clk}$

Reduction method:

Try to minimize

- ✓ Activity factor
- ✓ Capacitance
- ✓ Supply voltage

✓ Frequency $P_{total}=P_{dynamic}+P_{static}$

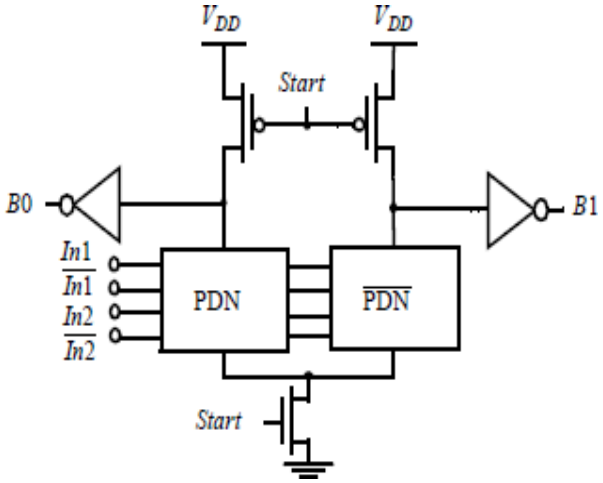
6. ***Explain about DCVSL logic with suitable example.*(Apr/May-17)**

- **Definition:*(2Marks)***

✓

- ✓ Differential Cascade Voltage Switch Logic consists of two parts–a complementary NMOS pull down network and PMOS load transistor.

- **Diagram:**



- **Explanation:**

- DCVSL is more expensive in terms of area than a non-redundant circuit due to its dual nature.
- It has advantage over static CMOS design in terms of circuit delay, layout area, logic flexibility and power dissipation.

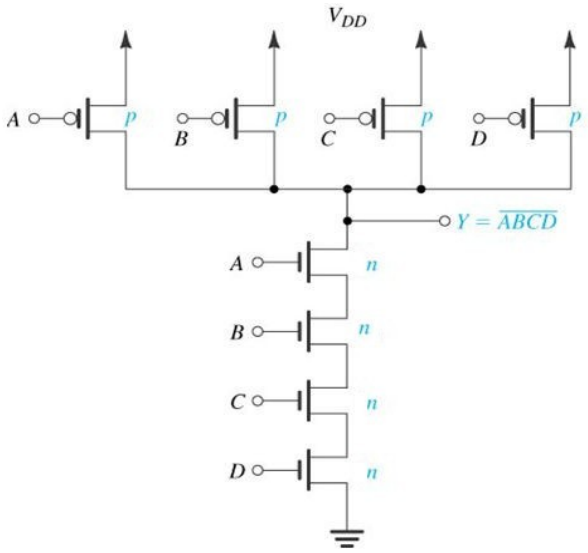
✓ `It has self testing property which can provide coverage for stuck-at fault and dynamic faults

7. Draw the static CMOS logic circuit for the following expression

(a) Y=(A.B.C.D)'

(b) Y=(D(A+BC))'**(May/Jun-16)**

(a) Y=(A.B.C.D)'



(b) Y=(D(A+BC))'