UNIT-2

ProgrammableDigitalSignalProcessors

3.1 Introduction:

Leadingmanufacturersofintegrated circuitssuch asTexas Instruments(TI),Analogdevices & Motorolamanufacturethedigitalsignalprocessor (DSP)chips.Thesemanufacturershavedevelopeda range of DSP chips with varied complexity.

The TMS320 family consists of two types of single chips DSPs: 16-bit fixed point &32-bit floating-point. These DSPs possess the operational flexibility of high-speed controllers and the numerical capability of array processors

3.2 CommercialDigitalSignal-ProcessingDevices:

ThereareseveralfamiliesofcommercialDSPdevices.Rightfromtheearlyeighties,whenthese devices began to appear in the market, they have been used in numerous applications, such as communication, control, computers, Instrumentation, and consumer electronics. The architectural featuresandtheprocessingpowerofthesedeviceshavebeenconstantlyupgradedbasedontheadvances in technology and the application needs. However, their basic versions, most of them have Harvard architecture, a single-cycle hardware multiplier, an address generation unit with dedicated address registers, special addressing modes, on-chip peripherals interfaces. Of the various families of programmableDSPdevicesthatarecommerciallyavailable,thethreemostpopularonesarethosefrom Texas Instruments, Motorola, and Analog Devices. Texas Instruments was one of the first to come out with a commercial programmable DSP with the introduction of its TMS32010 in 1982.

SummaryoftheArchitecturalFeaturesofthreefixed-PointsDSPs

Architectural Feature	TMS320C25	DSP 56000	ADSP2100
Data representation format	16-bit fixed	24-bit fixed point	16-bit fixed point
Hardware multiplier	16 x 16	24 x 24	16 x 16
ALU	32 bits	56 bits	40 bits
Internal buses	16-bit program bus	24-bit program bus	24-bit program bus
	16-bit data bus	2 x 24-bit data buses	16-bit data bus
		24-bit global	16-bit result

		databus	bus
External buses	16-bit program/data bus	24-bit program/data bus	24-bit program bus 16-bit data bus
On-chip Memory	544 words RAM 4K words ROM	512 words PROM 2 x 256 words data RAM 2 x 256 words data ROM	-
Off-chip memory	64 K words program 64k words data	64K words program 2 x 64K words data	16K words program 16K words data
Cache memory	-	-	16 words program
Instruction cycle time	100 nsec	97.5 nsec.	125 nsecc.
Special addressing modes	Bit reversed	Modulo Bit reversed	Modulo Bit reversed
Data address generators	1	2	2
Interfacing features	Synchronous serial I/O DMA	Synchronous and Asynchronous serial I/O DMA	DMA

3.3. ThearchitectureofTMS320C54xxdigitalsignalprocessors:

TMS320C54xx processors retain in the basic Harvard architecture of their predecessor, TMS320C25,buthaveseveraladditionalfeatures, whichimprovetheirperformanceoverit.Figure3.1 shows a functional block diagram of TMS320C54xx processors. They have one program and threedata memory spaces with separate buses, which provide simultaneous accesses to program instruction andtwodataoperandsandenableswritingofresultatthesametime.Partofthememoryisimplemented on-chip and consists of combinations of ROM, dual-access RAM, and single-access RAM. Transfers between the memory spaces are also possible.

Thecentral processingunit (CPU)ofTMS320C54xx processors consists ofa40- bit arithmetic logic unit (ALU), two 40-bit accumulators, a barrel shifter, a 17x17 multiplier, a 40-bit adder, data address generation logic (DAGEN) with its own arithmetic unit, and program address generation logic (PAGEN). These major functional units are supported by a number of registers and logic in the architecture. A powerful instruction set with a hardware-supported, single-instruction repeat and block repeat operations, block memory move instructions, instructions that pack two or three simultaneous reads, and arithmetic instructions with parallel store and load make these devices very efficient for running high-speed DSP algorithms.

Several peripherals, such as a clock generator, a hardwaretimer, a wait state generator, parallel I/O ports, and serial I/O ports, are also provided on-chip. These peripherals make it convenient to interface the signal processors to the outside world. In these following sections, we examine in detail the various architectural features of the TMS320C54xx familyof processors.

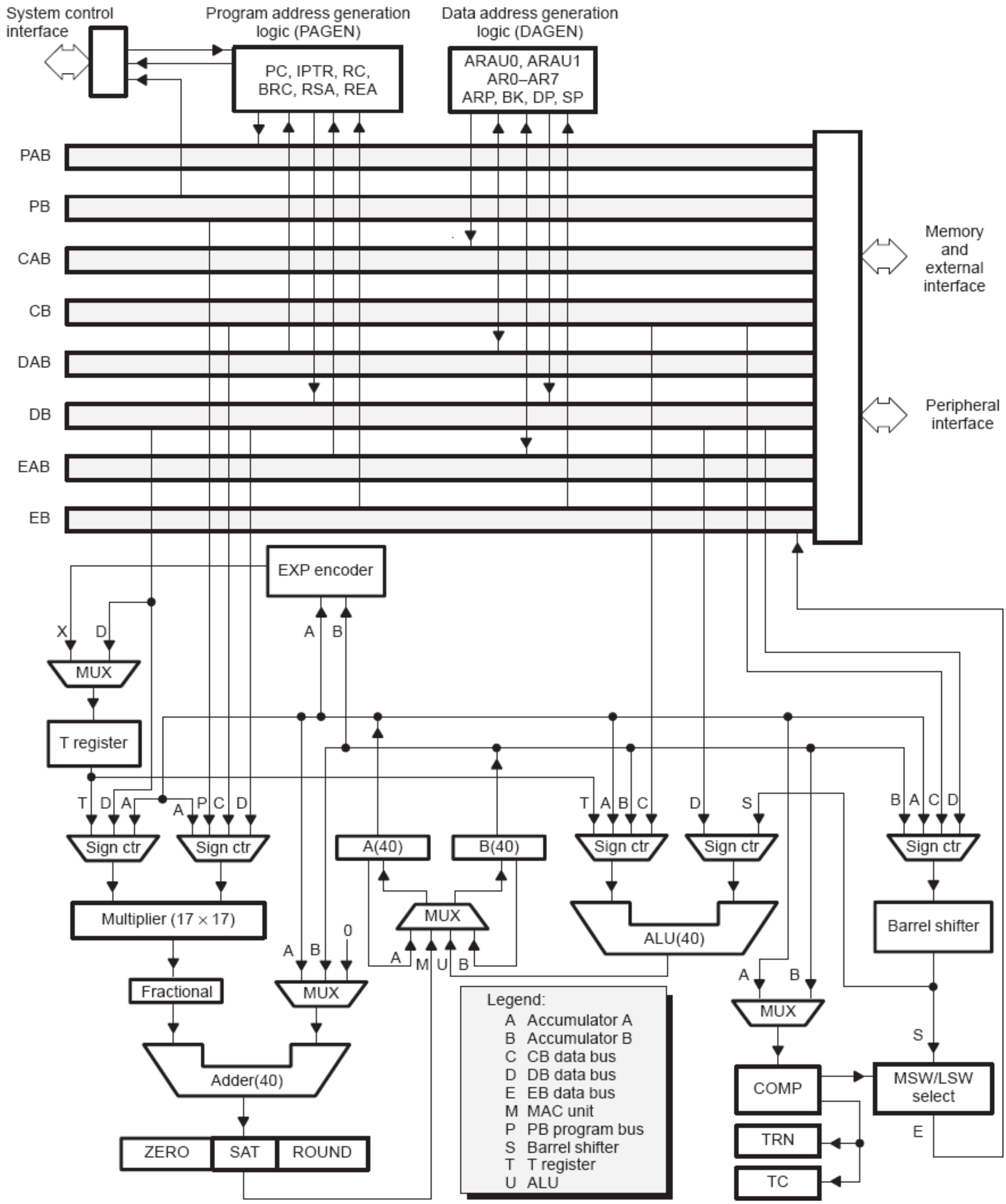


Figure3.1.FunctionalarchitectureforTMS320C54xxprocessors.

3.3.1 BusStructure:

The performance of a processor gets enhanced with the provision of multiple buses to provide simultaneous access to various parts of memory or peripherals. The 54xx architecture is built around fourpairsof16-bitbuseswitheachpairconsistingofanaddressbusandadatabus.Asshownin Figure

3.1, these are The program bus pair (**PAB, PB**); which carries the instruction code from the program memory.Threedatabuspairs(**CAB,CB;DAB,DB**;and**EAB,EB**);whichinterconnectedthevarious units within the CPU. In Addition the pair CAB, CB and DAB, DB are used to read from the data memory, while The pair **EAB, EB**; carries the data to be written to the memory. The ‘54xxcangenerate up to two data-memory addresses per cycle using the two auxiliary register arithmeticunit (ARAU0 and ARAU1) in the DAGEN block. This enables accessing two operands simultaneously.

3.3.2 CentralProcessingUnit(CPU):

The‘54xxCPUiscommontoallthe‘54xxdevices.The’54xxCPUcontainsa40-bitarithmetic logic unit (**ALU**); two 40-bit accumulators (**A** and **B**); a barrel shifter; a 17 x 17-bit multiplier; a 40-bit adder; a compare, select and store unit (**CSSU**); an exponent encoder(**EXP**); a data address generation unit (**DAGEN**); and a program address generation unit (**PAGEN**).

The ALU performs 2’s complement arithmetic operations and bit-level Boolean operations on 16, 32, and 40-bit words. It can also function as two separate 16-bit ALUs andperformtwo16-bitoperationssimultaneously. Figure3.2showthefunctionaldiagramoftheALU of the TMS320C54xx family of devices.

Accumulators A and B store the output from the ALU or the multiplier/adder block and provide a second input to the ALU. Each accumulators is divided into three parts: guards bits (bits 39-32), high-orderword(bits-31-16),andlow-orderword(bits15-0),whichcanbestoredandretrievedindividually. Each accumulator ismemory-mapped and partitioned. It can be configured as the destination registers. The guard bits are used as a head margin for computations.

AG(39-32)	AH(31-16)	AL(15-0)

BG(39-32)	BH(31-16)	BL(15-0)

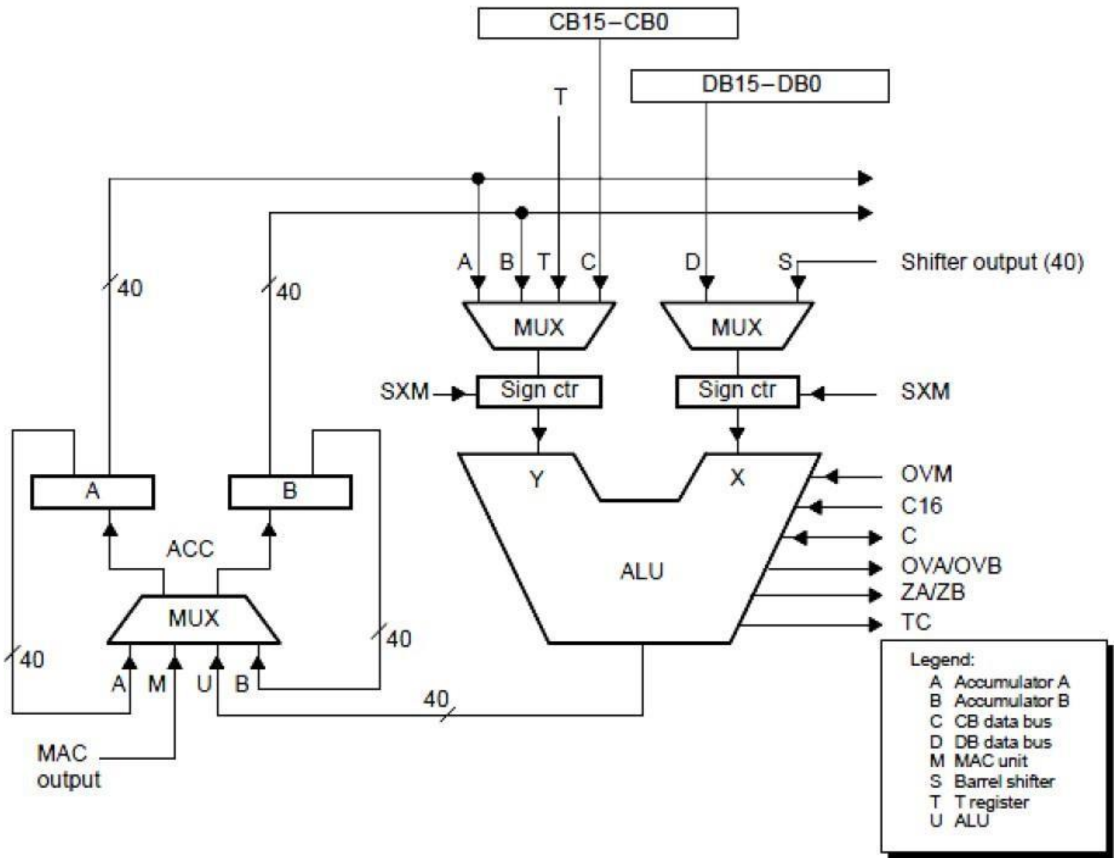


Figure3.2.Functionaldiagramofthe central processingunitofthe TMS320C54xxprocessors.

Barrel shifter:providesthecapabilitytoscalethedataduringanoperandreadorwrite. Nooverheadisrequiredtoimplementtheshiftneededforthescalingoperations.The'54xxbarrelshifter can produce a left shift of 0 to 31 bits or a right shift of 0 to 16 bits on the input data. The shift count field of status registers ST1, or in the temporary register T. Figure 3.3 shows the functional diagram of the barrel shifter of TMS320C54xx processors. The barrel shifter and the exponent encoder normalize the values in an accumulator in a single cycle. The LSBs of the output are filled with0s, and the MSBs can be either zero filled or sign extended, depending on the state of the sign-extension mode bit in the status register ST1. An additional shift capability enables the processor to perform numerical scaling, bit extraction, extended arithmetic, and overflow prevention operations.

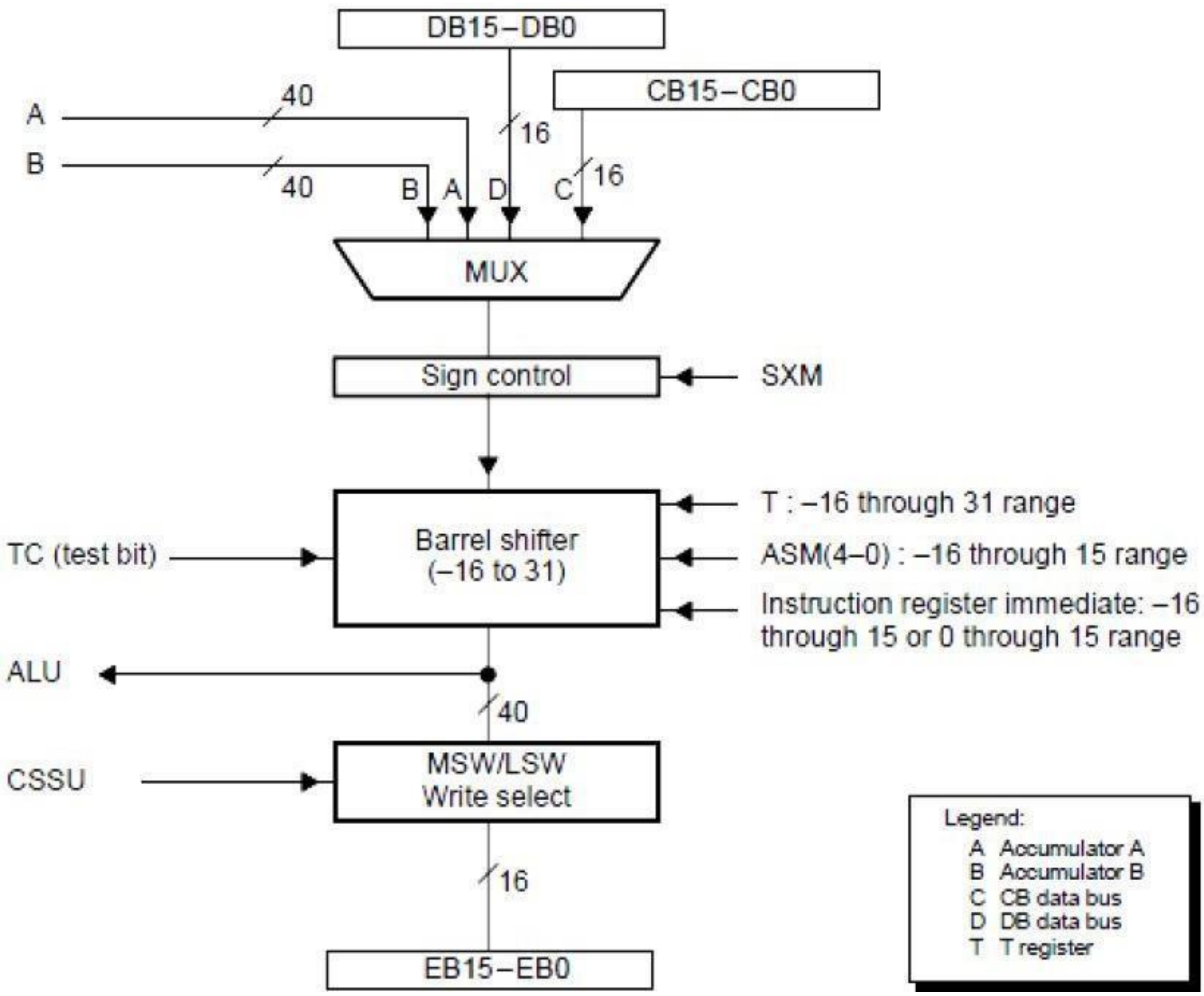


Figure3.3.Functionaldiagramofthebarrelshifter

Multiplier/adder unit: The kernel of the DSP device architecture is multiplier/adder unit. The multiplier/adder unit of TMS320C54xx devices performs 17 x 17 2's complement multiplication witha 40-bit addition effectively in a single instruction cycle.

Inadditiontothemultiplierandadder,theunitconsistsofcontrollogicforintegerandfractional computations and a16-bit temporarystorage register, T. Figure3.4 showthefunctional diagram ofthe multiplier/adder unit of TMS320C54xx processors. The compare, select, and store unit (CSSU) is a hardware unit specifically incorporated to accelerate the add/compare/select operation. This operation is essential to implement the *Viterbi* algorithm used in many signal-processing applications. The exponentencoderunitsupportstheEXPinstructions,whichstoresintheTregisterthenumberofleading redundant bits of the accumulator content. This information is useful while shifting the accumulator content for the purpose of scaling.

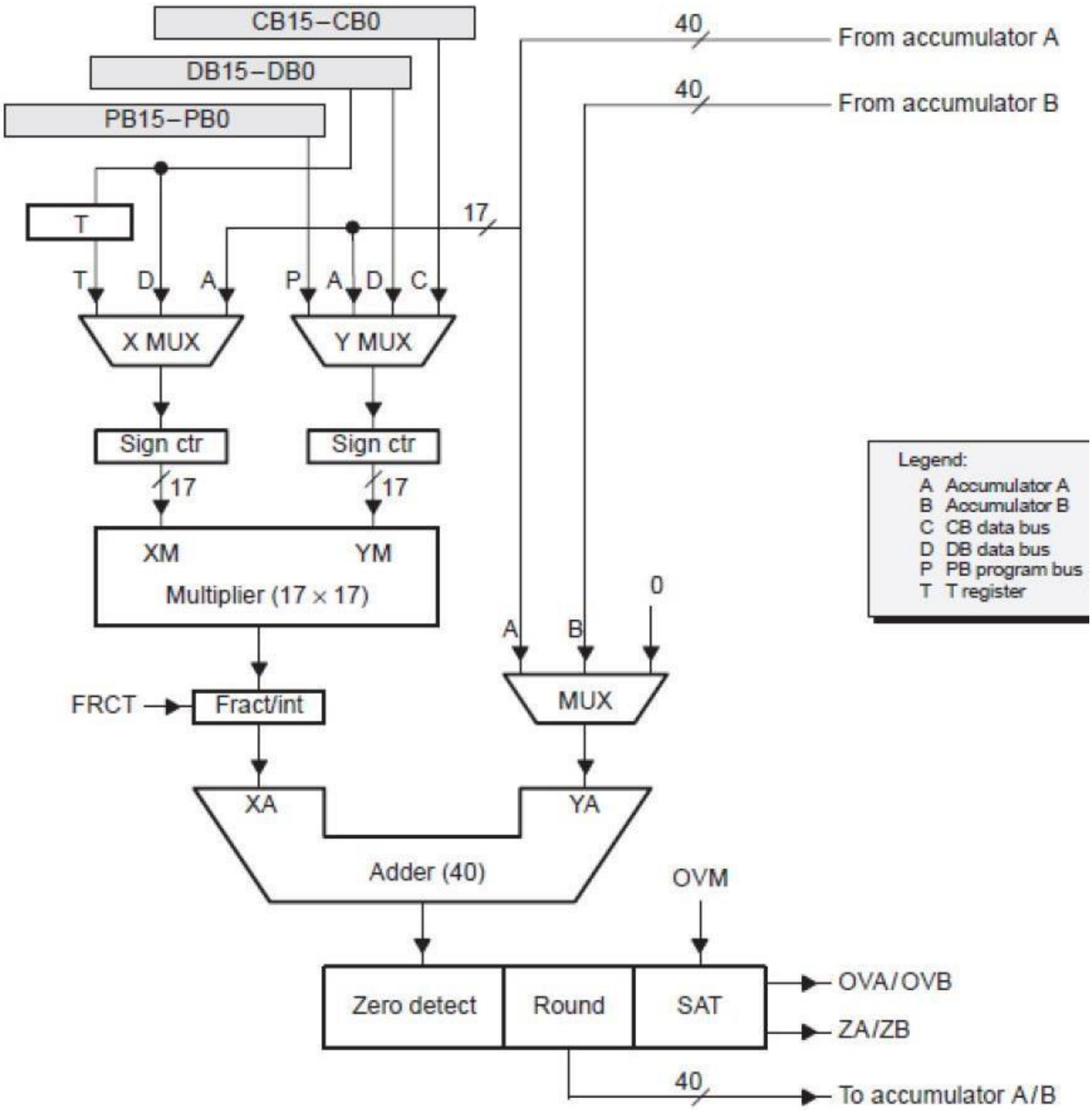


Figure3.4. Functionaldiagramofthemultiplier/adderunit ofTMS320C54xxprocessors.

3.3.3 InternalMemoryandMemory-MappedRegisters:

The amount and the types of memory of a processor have direct relevance to the efficiency and performance obtainable in implementations with the processors. The '54xx memory is organized into threeindividuallyselectablespaces:program,data,andI/Ospaces.All'54xxdevicescontainbothRAM andROM.RAMcanbeeitherdual-accesstype(DARAM)orsingle-accesstype(SARAM).Theon-chip RAM for these processors is organized in pages having 128 word locations on each page.

The'54xxprocessorshaveanumberofCPUregisterstosupportoperandaddressingandcomputations. TheCPUregistersandperipheralsregistersareallocatedonpage0ofthedatamemory.Figure 3.5(a) and (b) shows the internal CPU registers and peripheral registers with their addresses. The processors mode status (PMST) registers that is used to configure the processor. It is a memory-mapped register located at address 1Dh on page 0 of the RAM. A part of on-chip ROM maycontain a boot loader and look-up tables for function such as sine, cosine, μ- *law, and A*- law.

NAME	DEC	HEX	DESCRIPTION
IMR	0	0	Interrupt mask register
IFR	1	1	Interrupt flag register
—	2–5	2–5	Reserved for testing
ST0	6	6	Status register 0
ST1	7	7	Status register 1
AL	8	8	Accumulator A low word (15–0)
AH	9	9	Accumulator A high word (31–16)
AG	10	A	Accumulator A guard bits (39–32)
BL	11	B	Accumulator B low word (15–0)
BH	12	C	Accumulator B high word (31–16)
BG	13	D	Accumulator B guard bits (39–32)
TREG	14	E	Temporary register
TRN	15	F	Transition register
AR0	16	10	Auxiliary register 0
AR1	17	11	Auxiliary register 1
AR2	18	12	Auxiliary register 2
AR3	19	13	Auxiliary register 3
AR4	20	14	Auxiliary register 4
AR5	21	15	Auxiliary register 5
AR6	22	16	Auxiliary register 6
AR7	23	17	Auxiliary register 7
SP	24	18	Stack pointer register
BK	25	19	Circular buffer size register
BRC	26	1A	Block repeat counter
RSA	27	1B	Block repeat start address
REA	28	1C	Block repeat end address
PMST	29	1D	Processor mode status (PMST) register
XPC	30	1E	Extended program page register
—	31	1F	Reserved

Figure3.5(a) Internalmemory-mappedregistersofTMS320C54xxprocessors

NAME	ADDRESS DEC	HEX	DESCRIPTION
DRR20	32	20	McBSP 0 Data Receive Register 2
DRR10	33	21	McBSP 0 Data Receive Register 1
DXR20	34	22	McBSP 0 Data Transmit Register 2
DXR10	35	23	McBSP 0 Data Transmit Register 1
TIM	36	24	Timer Register
PRD	37	25	Timer Period Register
TCR	38	26	Timer Control Register
—	39	27	Reserved
SWWSR	40	28	Software Wait-State Register
BSCR	41	29	Bank-Switching Control Register
—	42	2A	Reserved
SWCR	43	2B	Software Wait-State Control Register
HPIC	44	2C	HPI Control Register (HMODE = 0 only)
—	45–47	2D–2F	Reserved
DRR22	48	30	McBSP 2 Data Receive Register 2
DRR12	49	31	McBSP 2 Data Receive Register 1
DXR22	50	32	McBSP 2 Data Transmit Register 2
DXR12	51	33	McBSP 2 Data Transmit Register 1
SPSA2	52	34	McBSP 2 Subbank Address Register
SPSD2	53	35	McBSP 2 Subbank Data Register
—	54–55	36–37	Reserved
SPSA0	56	38	McBSP 0 Subbank Address Register
SPSD0	57	39	McBSP 0 Subbank Data Register
—	58–59	3A–3B	Reserved
GPIOCR	60	3C	General-Purpose I/O Control Register
GPIOSR	61	3D	General-Purpose I/O Status Register
CSIDR	62	3E	Device ID Register
—	63	3F	Reserved
DRR21	64	40	McBSP 1 Data Receive Register 2
DRR11	65	41	McBSP 1 Data Receive Register 1
DXR21	66	42	McBSP 1 Data Transmit Register 2
DXR11	67	43	McBSP 1 Data Transmit Register 1
—	68–71	44–47	Reserved
SPSA1	72	48	McBSP 1 Subbank Address Register
SPSD1	73	49	McBSP 1 Subbank Data Register
—	74–83	4A–53	Reserved
DMPREC	84	54	DMA Priority and Enable Control Register
DMSA	85	55	DMA Subbank Address Register

Figure3.5(b).peripheralregistersfortheTMS320C54xxprocessors

Statusregisters(ST0,ST1):

ST0: Containsthestatusofflags(OVA,OVB,C,TC)producedbyarithmetic operations & bit manipulations.

ST1: Contain the status of various conditions & modes. Bits of ST0&ST1registers can be set or clear with the SSBX & RSBX instructions.

PMST: Containsmemory-setup status&controlinformation.

Status register0 diagram:

ARP	TC	C	OVA	OVB	DP
(15-13)	(12)	(11)	(10)	(9)	(8-0)

Figure3.6(a).ST0 diagram

ARP:Auxiliaryregisterpointer. TC:
Test/control flag.
C: Carrybit.
OVA:OverflowflagforaccumulatorA.
OVB: OverflowflagforaccumulatorB.
DP: Data-memory page pointer.

Status register1 diagram:

BRAF(15)	CPL	XF	HM	INTM	0	OVM	SXM	C16	FRCT(6)	CMPT(5)	ASM
	(14)	(13)	(12)	(11)	(10)	(9)	(8)	(7)			(4-0)

Figure3.6(b).ST1diagram

BRAF:Blockrepeatactiveflag

BRAF=0,theblockrepeatisdeactivated.
BRAF=1, the block repeat is activated.

CPL:Compilermode

CPL=0,therelativedirectaddressingmodeusingdatapagepointerisselected. CPL=1, the relative direct addressing mode using stack pointer is selected.

HM: Holdmode,indicateswhethertheprocessor continuesinternalexecutionoracknowledgefor external interface.

INTM:Interruptmode,itgloballymasksorenablesallinterrupts.

INTM=0_allunmaskedinterruptsareenabled.
INTM=1_all masked interrupts are disabled.
0: Always read as 0

OVM:Overflowmode.

OVM=1_thedestinationaccumulatorisseteitherthemostpositivevalueorthemostnegativevalue. OVM=0_the overflowed result is in destination accumulator.

SXM:Signextensionmode.

SXM=0_Signextensionissuppressed.

SXM=1_Data is sign extended

C16: Dual 16 bit/double-Precision arithmetic mode.
C16=0_ALUoperatesindouble-Precisionarithmeticmode.
C16=1_ALU operates in dual 16-bit arithmetic mode.

FRCT:Fractionalmode.

FRCT=1_themultiplieroutputisleft-shiftedby1bit to compensatean extrasign bit.

CMPT:Compatibilitymode.

CMPT=0_ARPisnotupdatedintheindirectaddressingmode. CMPT=1_ARP is updated in the indirect addressing mode.

ASM:AccumulatorShiftMode.

5bitfield,&specifiestheShiftvaluewithin-16to15 range.

ProcessorModeStatusRegister(PMST):

IPTR(15-7)	MP/MC(6)	OVLY(5)	AVIS(4)	DROM(3)	CLKOFF(2)	SMUL(1)	SST(0)

Figure 3.6(c).PMST register diagram

INTR: Interruptvectorpointer,pointtothe128-wordprogrampagewhere theinterruptvectors reside.
MP/MC:Microprocessor/Microcomputermode, MP/MC=0,
the on chip ROM is enabled.
MP/MC=1,theonchipROMis enabled.

OVLY: RAM OVERLAY, OVLY enables on chip dual access data RAM blocks to be mapped into program space.

AVIS: It enables/disablestheinternalprogramaddresstobevisibleattheaddress pins.
DROM:DataROM,DROMenableson-chipROMtobemappedintodataspace. CLKOFF: CLOCKOUT off.

SMUL:SaturationonMultiplication

SST:SaturationonStore.

3.4 DataAddressingModesofTMS320C54XProcessors:

Data addressing modes provide various ways to access operands to execute instructions and place results in the memoryor the registers. The 54XX devices offer seven basic addressing modes

1. Immediateaddressing.
2. Absoluteaddressing.
3. Accumulatoraddressing.
4. Directaddressing.
5. Indirectaddressing.
6. Memorymappedaddressing
7. Stackaddressing.

3.4.1 Immediateaddressing:

The instruction contains the specific value of the operand. The operand can be short (3,5,8 or 9 bitinlength)orlong(16bitsinlength).Theinstructionsyntaxforshortoperandsoccupiesonememory location,

Example:LD#20,DP.

RPT#0FFFFh.

3.4.2 AbsoluteAddressing:

Theinstructioncontainsaspecifiedaddressinthe operand.

1. Dmadaddressing.MVDKSmem,dmad,MVDMdmad,MMR
2. Pmadaddressing.MVDPSmem,pmad,MVPDpmem,Smad
3. PAaddressing.PORTRPA,Smem,
4. *(lk)addressing.

3.4.3 AccumulatorAddressing:

AccumulatorcontentisusedasaddresstotransferdatabetweenProgramandData memory.

Ex:READA*AR2

3.4.4 DirectAddressing:

Baseaddress+7bitsofvaluecontainedininstruction=16bitaddress.Apageof128locations can be accessed without change in DP or SP.Compiler mode bit (CPL) in ST1 register is used.

IfCPL=0SelectsDP

CPL = 1 selects SP,

It shouldberememberedthat whenSPisusedinsteadofDP,theeffectiveaddressiscomputed byaddingthe7-bit offsetto SP

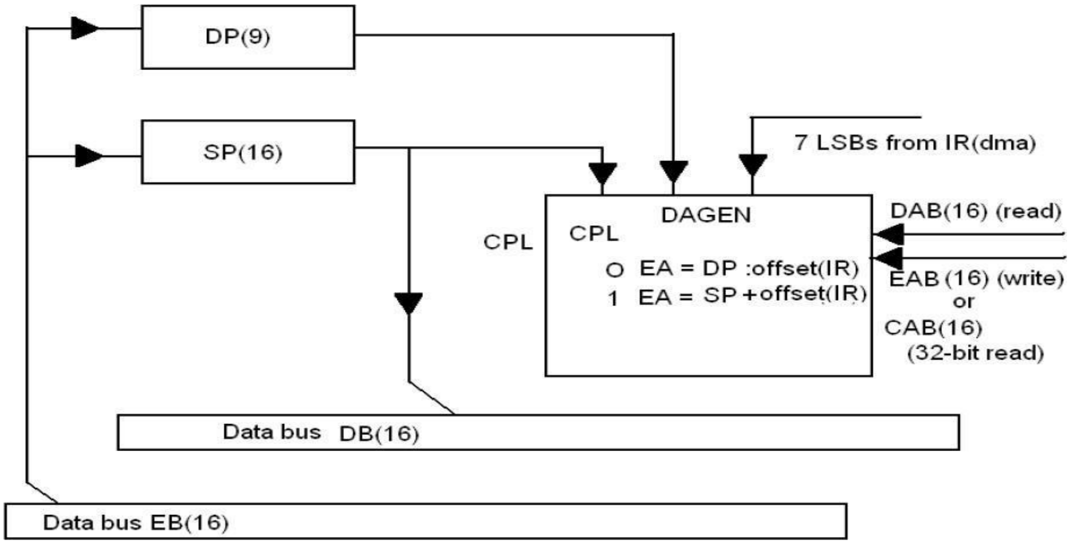


Figure3.7Blockdiagram ofthedirectaddressingmodeforTMS320C54xxProcessors.

3.4.1IndirectAddressing:

Data space is accessed by address present in an auxiliary register.

TMS320C54xx have 8, 16 bit auxiliaryregister (AR0 – AR 7). Two auxiliaryregister arithmetic units (ARAU0 & ARAU1)

Usedtoaccessmemorylocationinfixedstepsize.AR0registerisusedforindexedandbitreverse addressing modes.

For single – operand addressing

MOD_typeofindirectaddressing

ARF _ AR used for addressing

ARP dependson(CMPT)bitin ST1

CMPT=0, Standardmode,ARPsetto zero

CMPT=1,Compatibilitymode,ParticularlyARselected byARP

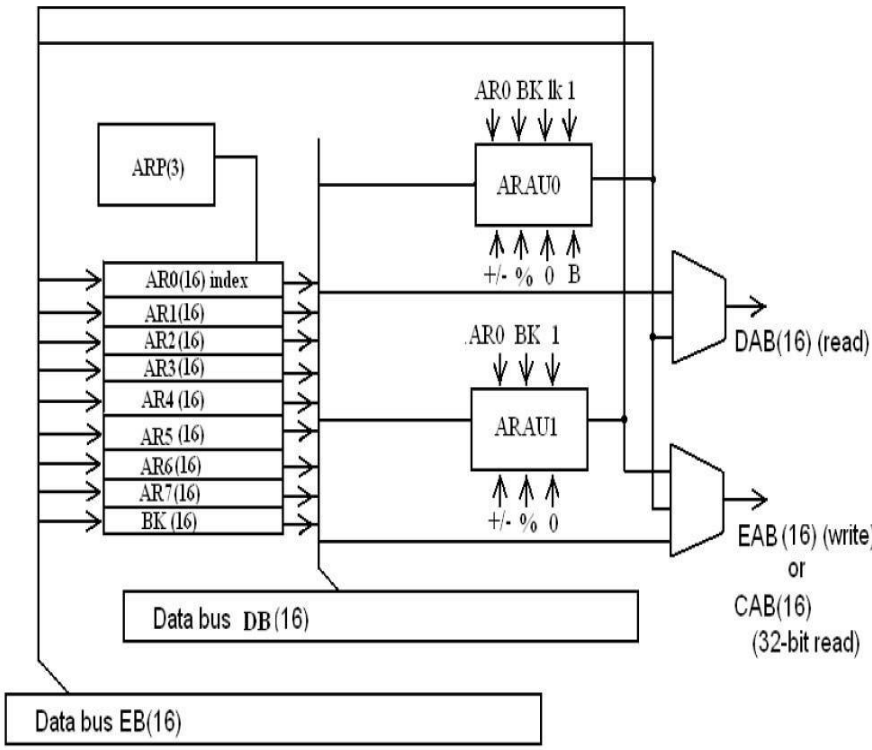


Figure 3.8 Block diagram of the indirect addressing mode for TMS320C54xx Processors.

Operand syntax	Function
*ARx	Addr = ARx;
*ARx -	Addr = ARx ; ARx = ARx -1
*ARx +	Addr = ARx; ARx = ARx +1
*+ARx	Addr = ARx+1; ARx = ARx +1
*ARx - 0B	Addr = ARx ; ARx = B(ARx – AR0)
*ARx - 0	Addr = Arx ; ARx = ARx – AR0
*ARx + 0	Addr = Arx ; ARx = ARx +AR0
*ARx + 0B	Addr = ARx ; ARx = B(ARx + AR0)
*ARx - %	Addr = ARx ; ARx = circ(ARx – 1)
*+AR – 0%	Addr = Arx; ARx = circ(ARx - AR0)
*ARx + %	Addr = ARx ; ARx = circ (ARx + 1)

Table3.2 Indirectaddressingoptionswithasingle data–memoryoperand.

CircularAddressing;

- Usedinconvolution,correlationandFIRfilters.
- Acircularbufferisaslidingwindowcontainsmostrecentdata.CircularbufferofsizeRmust start on a N-bit boundary, where 2N > R .
- The circular buffer size register (BK): specifies the size of circular buffer.
- Effectivebaseaddress(EFB):ByzeroingtheNLSBsofauserselectedAR (ARx).
- End of buffer address (EOB) : By repalcing the N LSBs of ARx with the N LSBs of BK.
  If0 _ index+step <BK; index=index+step;
  elseif index+step _BK; index=index+step-BK;

elseif index+step<0;index+step+BK

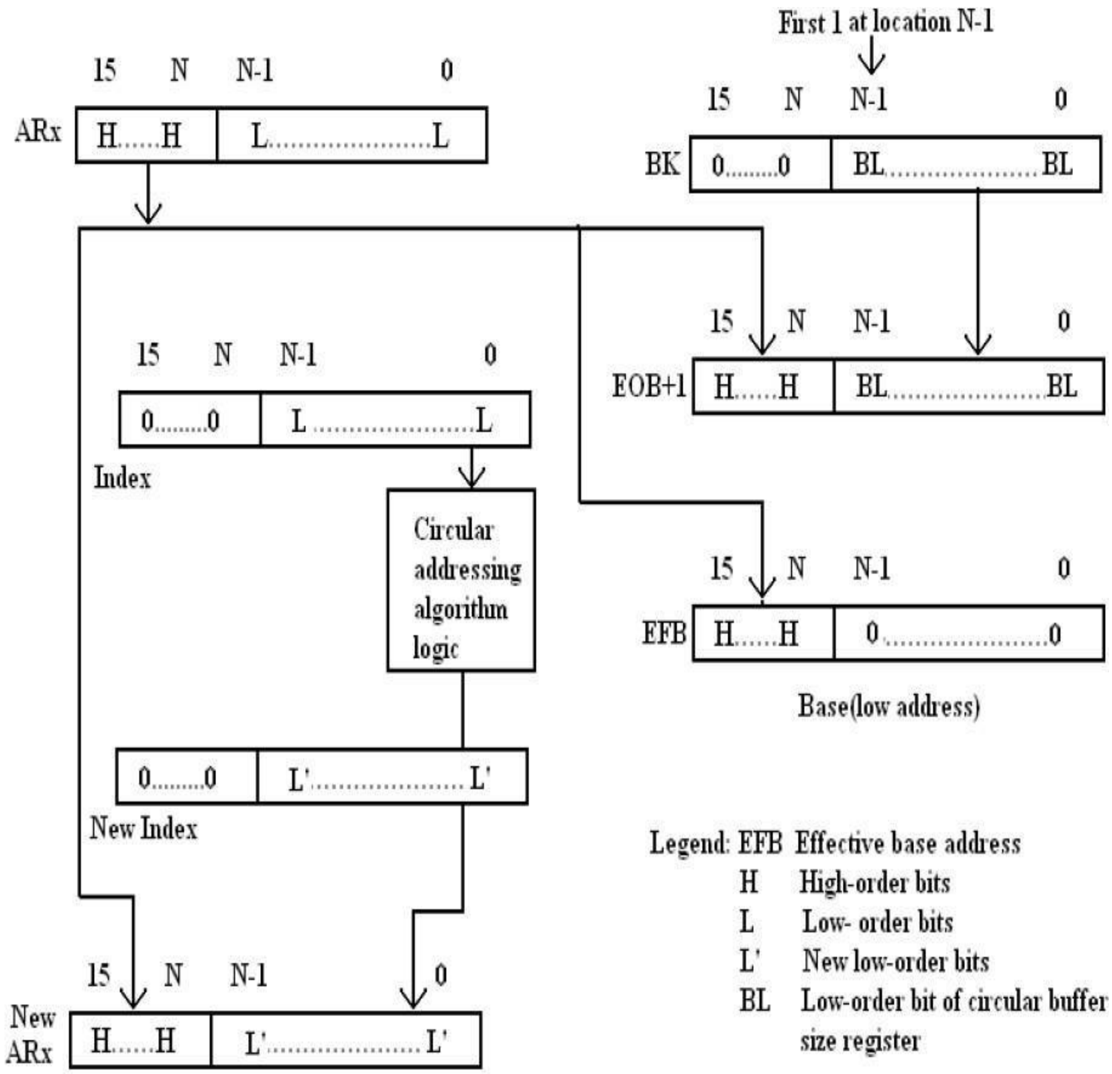


Figure 3.9 Block diagram of the circular addressing mode for TMS320C54xx Processors.

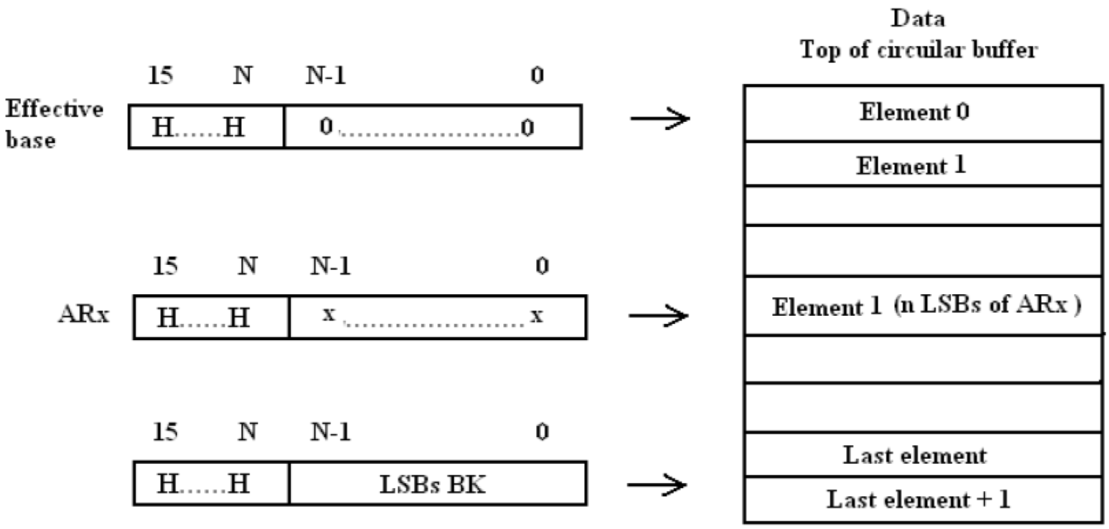


Figure 3.10 circular addressing mode implementation for TMS320C54xx Processors.

Bit-ReversedAddressing:

- UsedforFFT algorithms.
- AR0specifiesonehalf ofthesizeofthe FFT.
- Thevalueof AR0=2N-1:N=integerFFTsize= 2N
- AR0+AR(selectedregister)=bitreverseaddressing.
- Thecarrybitpropagatingfromlefttoright.

Dual-OperandAddressing:

Dualdata-memoryoperandaddressingisusedforinstructionthatsimultaneously perform two reads (32-bit read) or a single read (16-bit read) and a parallel store (16-bit store) indicated by two vertical bars, II. These instructions access operands using indirect addressing mode.

If in an instruction with a parallel store the source operand the destination operand point to the same location, the source is read before writing to the destination. Only 2 bits are available in the instruction code for selecting each auxiliary register in this mode. Thus, just four of the auxiliary registers,AR2-AR5,canbeused,TheARAUstogetherwiththeseregisters,providecapabilitytoaccess twooperandsinasinglecycle.Figure3.11showshowanaddressisgeneratedusingdualdata-memory operand addressing.

15 - 8	7 - 6	5 - 4	3 - 2	1 - 0
Opcode	Xmod	Xar	Ymod	Yar

Name	Function
Opcode	This field contains the operation code for the instruction
Xmod	Defined the type of indirect addressing mode used for accessing the Xmem operand
XAR	Xmem AR selection field defines the AR that contains the address of Xmem
Ymod	Defies the type of inderect addressing mode used for accessing the Ymem operand
Yar	Ymem AR selection field defines the AR that contains the address of Ymem

Table 3.3.Function of the different field in dual data memory operand addressing

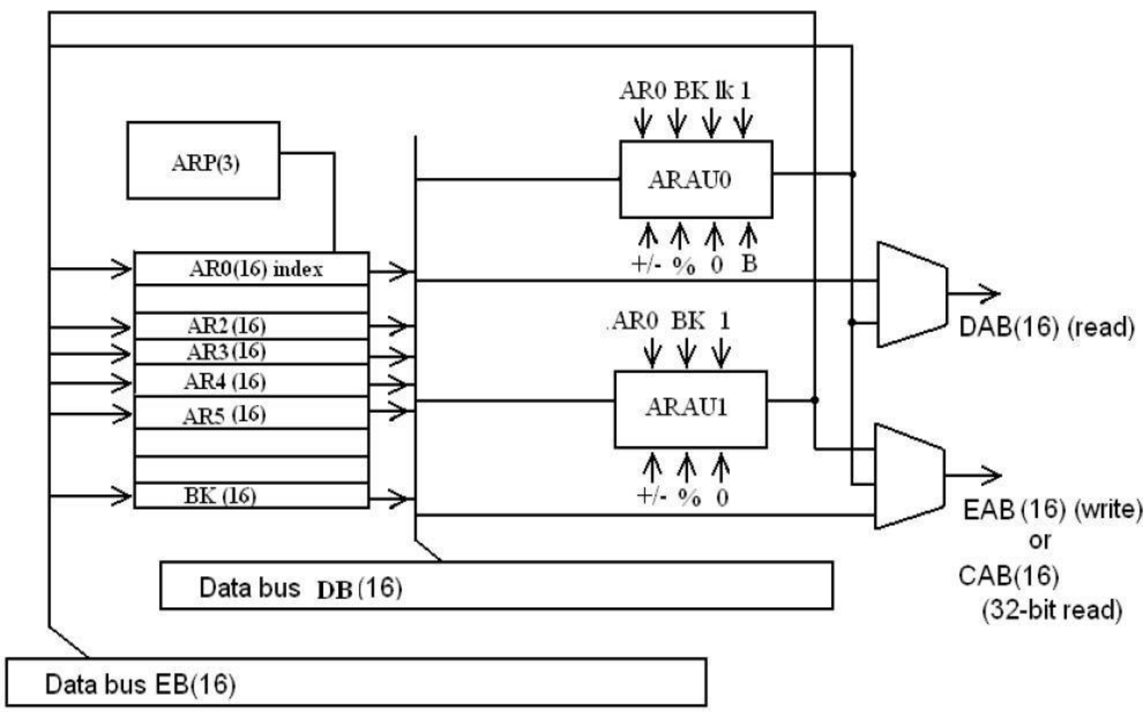


Figure 3.11 Block diagram of the Indirect addressing options with a dual data –memory operand.

3.4.6.Memory-MappedRegisterAddressing:

- Usedtomodifythememory-mappedregisterswithoutaffectingthecurrentdata page
- pointer(DP)orstack-pointer(SP)
  - Overheadforwritingtoaregisterisminimal
  - Worksfordirectandindirect addressing
  - Scratch–padRAMlocatedondataPAGE0 canbemodified
- STM#x, DIRECT
- STM#tbl,AR1

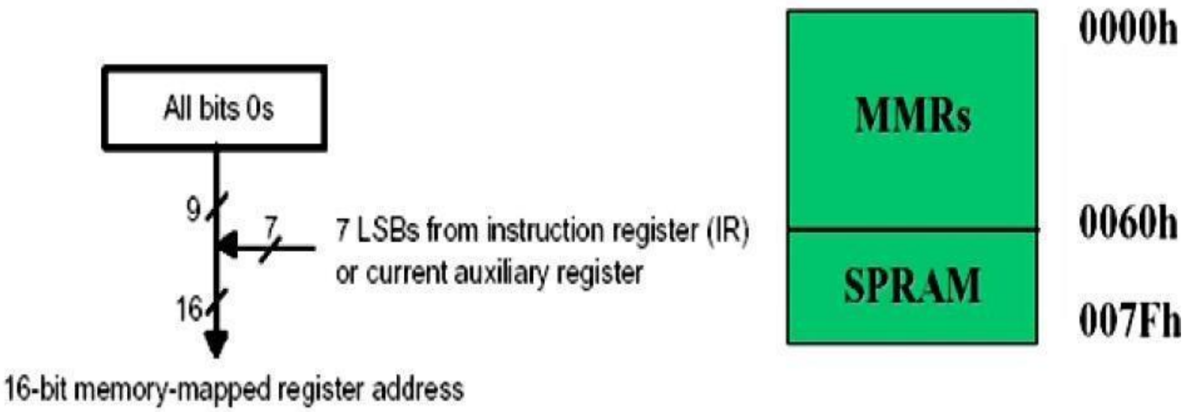


Figure 3.12.16 bit memory mapped register address generation.

3.4.7StackAddressing:

- Usedtoautomaticallystoretheprogramcounterduringinterruptsandsubroutines.
- Canbeusedtostoreadditionalitemsofcontextortopassdatavalues.
- Usesa16-bitmemory-mappedregister,thestackpointer(SP).
- PSHDX2

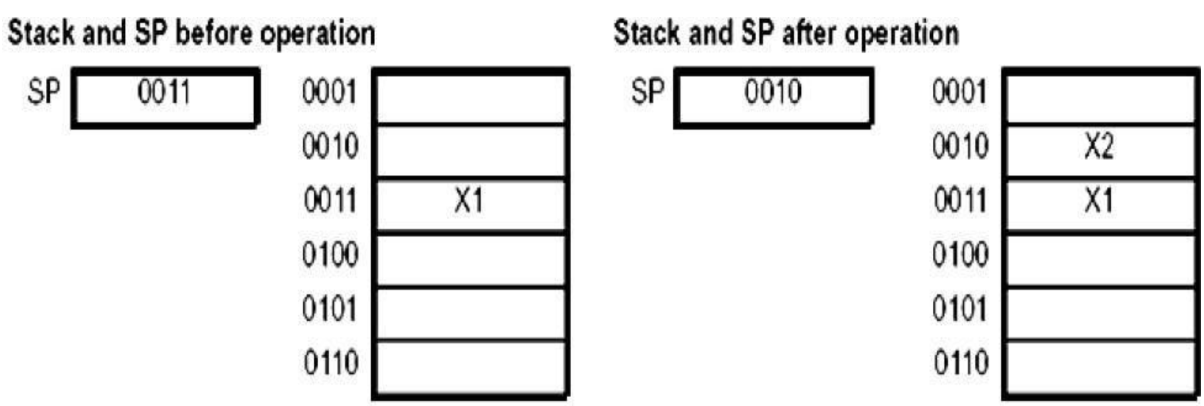
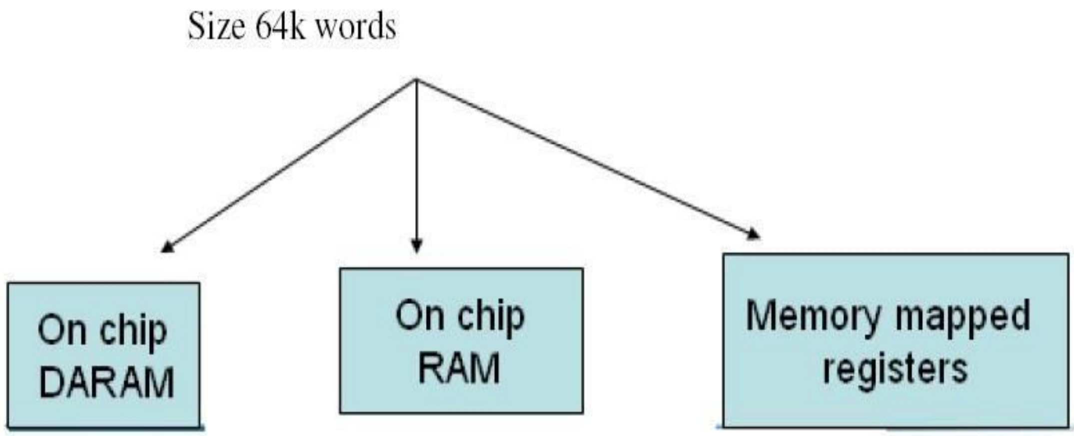


Figure 3.13. Values of stack &SP before and after operation.

3.5.MemorySpaceofTMS320C54xxProcessors

- Atotalof128kwordsextendableupto8192kwords.
- TotalmemoryincludesRAM,ROM,EPROM,EEPROMorMemorymappedperipherals.
- Data memory: To store data required to run programs & for external memorymapped registers.



Program memory: To store program instructions &tables used in the execution of programs.

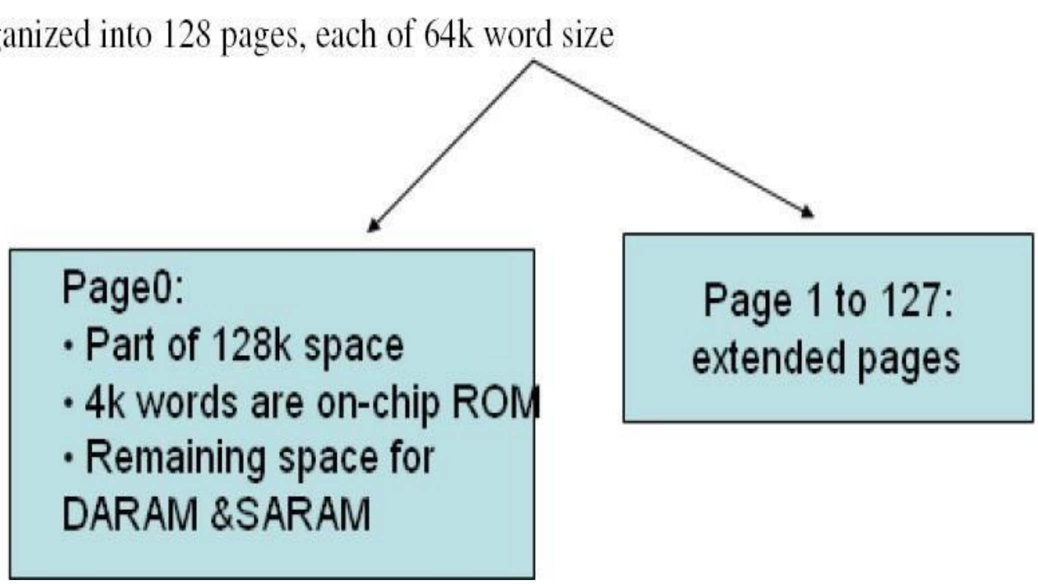
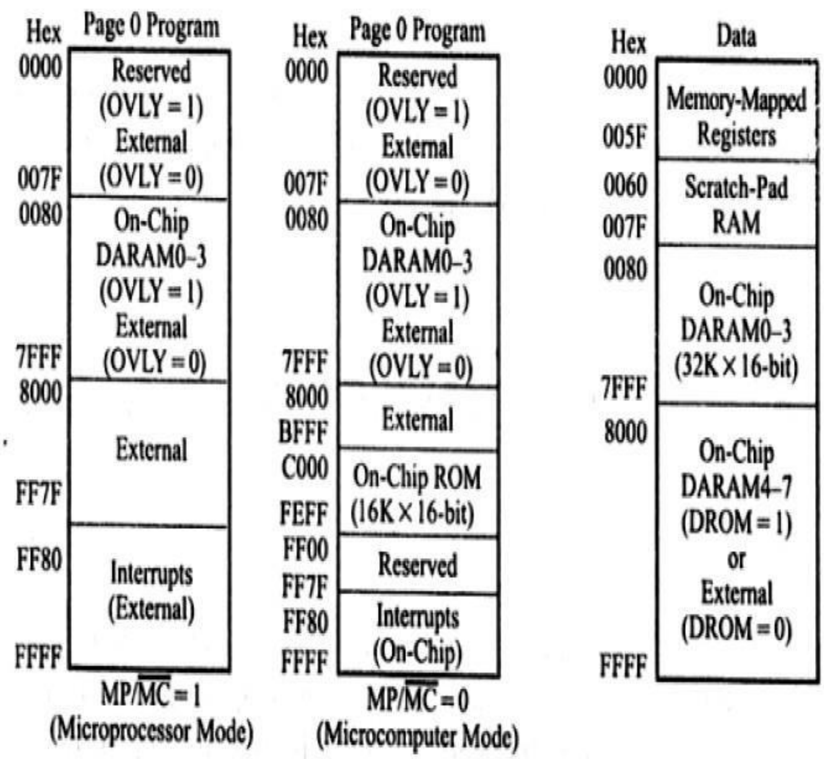


Table 3.4.Function of different pin PMST register

PMST bit	Logic	On-chip memory configuration
MP/MC	0 1	ROM enabled ROM not available
OVLY	0 1	RAM in data space RAM in program space
DROM	0 1	ROM not in data space ROM in data space



Address ranges for on-chip DARAM in data memory are: DARAM0: 0080h–1FFFh; DARAM1: 2000h–3FFFh; DARAM2: 4000h–5FFFh; DARAM3: 6000h–7FFFh; DARAM4: 8000h–9FFFh; DARAM5: A000h–BFFFh; DARAM6: C000h–DFFFh; DARAM7: E000h–FFFFh

Figure3.14 Memorymap forthe TMS320C5416Processor.

3.6.ProgramControl

- It contains program counter (PC), the program counter related H/W, hard stack, repeat counters &status registers.
- PCaddressesmemoryinseveralwaysnamely:
- Branch:ThePCisloadedwiththeimmediatevaluefollowingthebranch instruction
- Subroutinecall:ThePCisloadedwiththeimmediatevaluefollowingthe callinstruction
- Interrupt:ThePCisloadedwiththeaddressoftheappropriateinterrupt vector.
- Instructionssuch as BACC, CALA, etc ;ThePC is loaded with the contentsofthe accumulator low word
- Endofablockrepeatloop:The PCisloadedwiththecontentsoftheblockrepeat programaddress start register.
- Return:ThePCisloadedfromthetopofthe stack.

Problems:

1. Assuming the current content of AR3 to be 200h, what will be its contents aftereachofthefollowingTMS320C54xxaddressingmodesisused?Assumethatthe contents of AR0 are 20h.

a. *AR3+0
b. *AR3-0
c. *AR3+
d. *AR3
e. *AR3
f. *+AR3(40h)
g. *+AR3(-40h)

Solution:

a. AR3 ←AR3 +AR0;AR3
=200h+20h= 220h
b. AR3←AR3-AR0;
AR3=200h-20h=1E0h
c. AR3 ←AR3 +1;AR3
=200h+1= 201h
d. AR3 ←AR3-1;AR3
=200h-1= 1FFh
e. AR3 isnot modified.
AR3 =200h
f. AR3←AR3 +40h;AR3
=200+40h= 240h
g. AR3←AR3-40h;AR3
=200-40h=1C0h

2. Assumingthecurrentcontentsof AR3tobe200h,whatwillbeitscontents after eachofthefollowingTMS320C54xxaddressingmodesisused?Assumethat the contents of AR0 are20h

a. *AR3+0B

b. *AR3–0B

Solution:

a. AR3 ← AR3 + AR0 with reverse carrypropagation;AR3=200h+20h (with reverse carry propagation) = 220h.

b. AR3 ← AR3 - AR0 with reverse carrypropagation;AR3=200h-20h (with reverse carry propagation) = 23Fh.

3.7 Onchipperipherals:

Itfacilitatesinterfacingwithexternaldevices.Theperipheralsare:

- GeneralpurposeI/Opins
- Asoftwareprogrammable waitstate generator.
- Hardwaretimer
- Hostportinterface(HPI)
- Clockgenerator
- Serialport

3.7.1 IthastwogeneralpurposeI/Opins:

- BIO-inputpinusedtomonitorthestatusofexternaldevices.
- XF-outputpin,softwarecontrolledusedtosignalexternaldevices

3.7.2 Softwareprogrammablewaitstategenerator:

- Extendsexternalbuscyclesuptosevenmachinecycles.

3.7.3 HardwareTimer

- An on chip down counter
- Used to generate signal to initiate any interrupt or any other process

Consistsof3 memorymappedregisters:

- Thetimerregister (TIM)
- Timerperiodregister (PRD)
- Timercontrolsregister(TCR)
  - Prescalerblock (PSC).
  - TDDR(TimeDivideDown ratio)
  - TIN&TOUT

The timer register (TIM) is a 16-bit memory-mapped register that decrements at every pulse from the prescaler block (PSC).
Thetimerperiodregister(PRD)isa16-bitmemory-mappedregisterwhose contentsareloadedontotheTIMwhenevertheTIMdecrementstozeroorthe

deviceis reset (SRESET).

Thetimercanalsobeindependentlyresetusingthe TRBsignal.Thetimer controlregister(TCR)isa16-bitmemory-mappedregisterthatcontainsstatusand control bits. Table shows the functions of the various bits in the TCR.

Theprescalerblockisalsoanon-chipcounter.Whenevertheprescalerbits count down to 0, a clock pulse is given to the TIM register that decrements the TIMregisterby1.TheTDDRbitscontain thedivide-downratio,whichisloaded onto the prescaler block after each time the prescaler bits count down to 0.

That is to saythat the 4-bit value of TDDR determines the divide-by ratio of the timer clock with respect to the system clock. In other words, the TIM decrements either at the rate of the system clock or at a rate slower than that as decided by the value of the TDDR bits. TOUT and TINT are the output signal generated as the TIM register decrements to 0. TOUT can trigger the start of the conversion signal in an ADC interfaced to the DSP.

ThesamplingfrequencyoftheADCdetermineshowfrequentlyitreceives theTOUTsignal.TINTisusedtogenerateinterrupts,whicharerequiredtoservice a peripheral such as a DRAM controller periodically. The timer can also be stopped, restarted, reset, or disabled by specific status bits.

Bit	Name	Function
15-12	Reserved	Reserved; always read as 0.
11	Soft	Used in conjunction with the free bit to determine the state of the timer Soft=0,the timer stops immediately. Soft=1,the timer stops when the counter decrements to 0.
10	Free	Use in conjunction with the soft bit Free=0,the soft bit selects the timer mode free=1,the timer runs free
Bit	Name	Function
9-6	PSC	Timer prescaler counter, specifies the count for the on-chip timer
5	TRB	Timer reload. Reset the on-chip timer.
4	TSS	Timer stop status, stop or starts the on-chip timer.
3-0	TDDR	Timer divide-down ration

Table 4.6. Pin details of software wait state generator

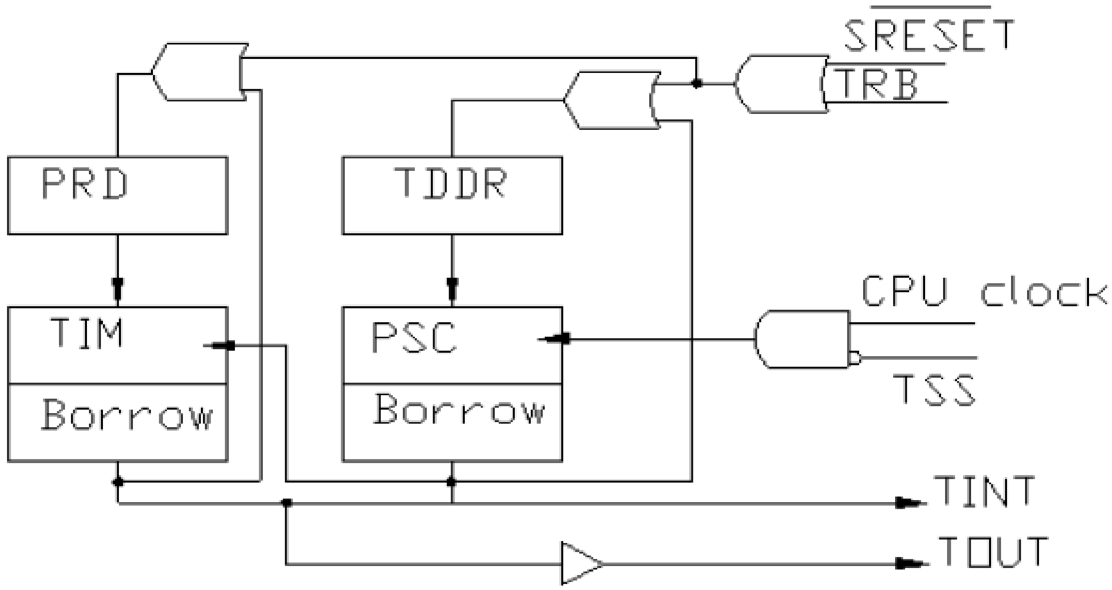


Figure 4.2.Logical block diagram of timer circuit.

3.8 InterruptsofTMS320C54xxProcessors:

Manytimes,whenCPUisinthemidstofexecutingaprogram,aperipheral device mayrequirea service from the CPU. In such a situation, the main program maybeinterruptedbyasignal generatedbytheperipheraldevices.This resultsin the processor suspending the main programin order to execute another program, calledinterruptserviceroutine,toservicetheperipheraldevice.On completionof theinterruptserviceroutine,theprocessorreturnstothemainprogramtocontinue fromwhere it left.

Interrupt maybe generated eitherbyan internal oran external device. It mayalso be generated by software. Not all interrupts are serviced when they occur. Only those interrupts that are called *nonmaskable* are serviced whenever they occur. Otherinterrupts,whicharecalled*maskable*interrupts,areservicedonlyiftheyare enabled. There is also a priority to determine which interrupt gets servicedfirst if more than one interrupts occur simultaneously.

Almostallthedevicesof TMS320C54xx familyhave32interrupts.However,the types and the number under each type vary from device to device. Some of these interruptsare reserved for use by the CPU.

3.9 PipelineoperationofTMS320C54xxProcessors:

The CPU of ‘54xx devices have a six-level-deep instruction pipeline. The six stages of the pipeline are independent of each other. This allows overlapping execution of instructions. During any given cycle, up to six different instructions canbeactive,eachatadifferentstageofprocessing.Thesixlevelsofthepipeline structure are program prefetch, program fetch, decode, access, read and execute.1

During program prefetch, the program address bus, PAB, is loaded with theaddress of the next instruction to be fetched.

2 In the fetch phase, an instruction word is fetched from the program bus, PB, andloadedintotheinstructionregister,IR.Thesetwophasesfromtheinstruction fetchsequence.

3 During the decode stage, the contents of the instruction register, IR are decoded to determine thetype of memory access operation and the control signals required for the data-address generation unit and the CPU.

4 The access phase outputs the read operand’s on the data address bus, DAB. If asecondoperandis required,theotherdataaddressbus,CAB, alsoloadedwith anappropriate address. Auxiliary registers in indirect addressing mode and the stack pointer (SP) are also updated.

5 Inthereadphasethedataoperand(s),ifany,arereadfromthedatabuses,DB and CB. This phase completes the two-phase read process and starts the two phase write processes. The data address of thewrite operand, if any, is loaded into the data write address bus, EAB.

6 Theexecutephasewritesthedatausingthedatawritebus,EB,andcompletes the

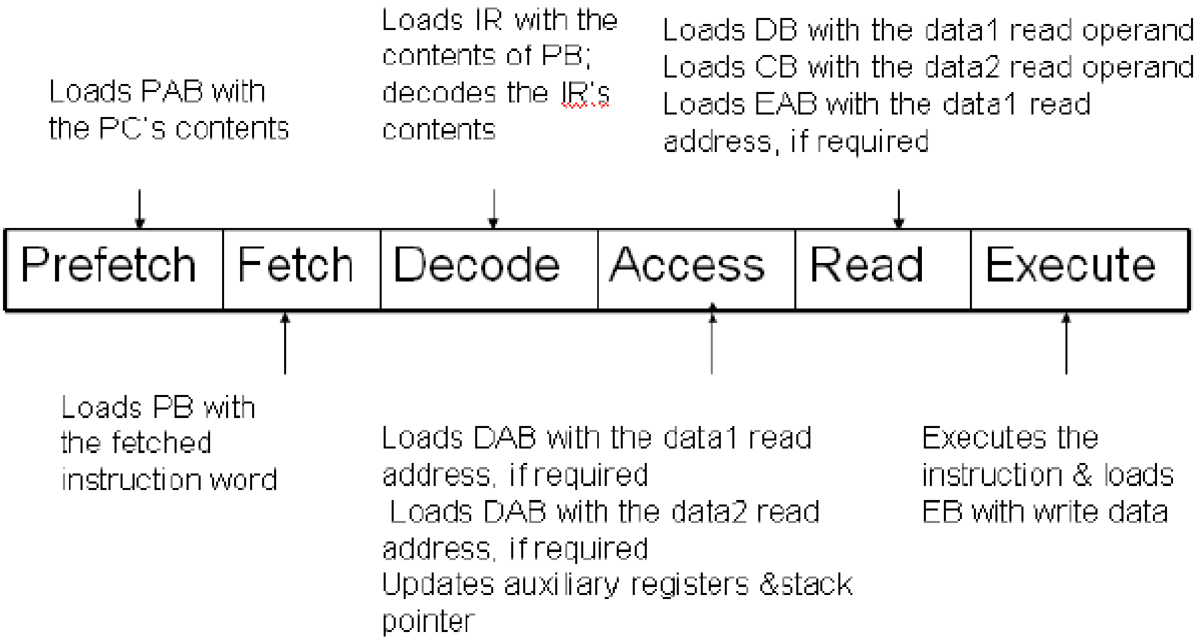


Figure 4.4. Pipeline operation of TMS320C54xx Processors

Pipe Flow

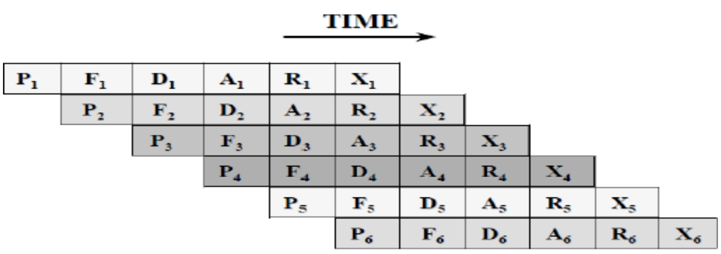


Figure 4.5.Pipe flow diagram

operand write sequence. The instruction is executed in phase