



Unit III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS

1. Properties of feedback circuits.

Gain Desensitization Consider the common-source stage, where the voltage gain is equal to $g_{m1}r_{O1}$. A critical drawback of this circuit is the poor definition of the gain: both g_{m1} and r_{O1} vary with process and temperature. Now suppose the circuit is configured as in (b), where the gate bias of M_1 is set by means not shown here. Let us calculate the overall voltage gain of the circuit at relatively low frequencies such that C_2 draws a negligible (small-signal) current from the output node, i.e., $V_{out}/V_X = -g_{m1}r_{O1}$ because the entire drain current flows through r_{O1} . Since $(V_{out} - V_X)C_2s = (V_X - V_{in})C_1s$, we have

$$\frac{V_{out}}{V_{in}} = -\frac{1}{\left(1 + \frac{1}{g_{m1}r_{O1}}\right) \frac{C_2}{C_1} + \frac{1}{g_{m1}r_{O1}}} \quad (8.3)$$

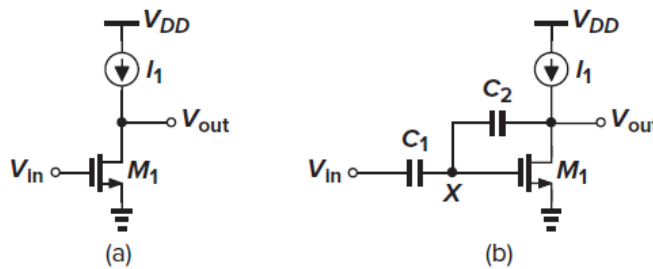


Figure 8.3 (a) Simple common-source stage; (b) circuit of (a) with feedback.

If $g_{m1}r_{O1}$ is sufficiently large, the $1/(g_{m1}r_{O1})$ terms in the denominator can be neglected, yielding

$$\frac{V_{out}}{V_{in}} = -\frac{C_1}{C_2}$$

Compared to $g_{m1}r_{O1}$, this gain can be controlled with much higher accuracy because it is given by the ratio of two capacitors. If C_1 and C_2 are made of the same material, then process and temperature variations do not change C_1/C_2 .

The above example reveals that negative feedback provides gain “desensitization,” i.e., the closed-loop gain is less sensitive to device parameters than the open-loop gain is. One may also say that negative feedback “stabilizes” the gain and hence “improves the stability.” But this nomenclature may be confused with frequency stability (Chapter 10), which typically *worsens* as a result of negative feedback. Illustrated for a more general case in Fig. 8.4, gain desensitization can be quantified by writing

$$\frac{Y}{X} = \frac{A}{1 + \beta A} \quad (8.5)$$

$$\approx \frac{1}{\beta} \left(1 - \frac{1}{\beta A}\right) \quad (8.6)$$

where we have assumed that $\beta A \gg 1$. We note that the closed-loop gain is determined, to the first order by the feedback factor, β . More important, even if the open-loop gain, A , varies by a factor of, say, 2, Y/X varies by a small percentage because $1/(\beta A) \ll 1$.

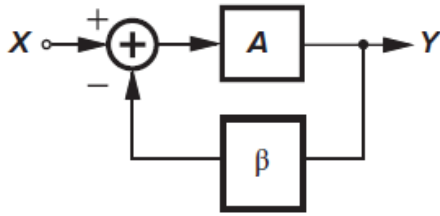


Figure 8.4 Simple feedback system.

Called the “loop gain,” the quantity βA plays an important role in feedback systems.¹ We see from (8.6) that the higher βA is, the less sensitive Y/X will be to variations in A . From another perspective, the accuracy of the closed-loop gain improves by maximizing βA . Note that as β increases, the closed-loop gain, $Y/X \approx 1/\beta$, decreases, suggesting a trade-off between precision and the closed-loop gain. In other words, we begin with a high-gain amplifier and apply feedback to obtain a low, but less sensitive, closed-loop gain. Another conclusion here is that the output of the feedback network is equal to $\beta Y = X \cdot \beta A / (1 + \beta A)$, approaching X as βA becomes much greater than unity.

Terminal Impedance Modification As a second example, let us study the circuit shown in Fig. 8.8(a), where a capacitive voltage divider senses the output voltage of a common-gate stage, applying the result to the gate of current source M_2 and hence returning a signal to the input.³ Our objective is to compute the input resistance at relatively low frequencies with and without feedback. Neglecting channel-length modulation and the current drawn by C_1 , we break the feedback loop as shown in Fig. 8.8(b) and write

$$R_{in,open} = \frac{1}{g_{m1} + g_{mb1}} \quad (8.9)$$

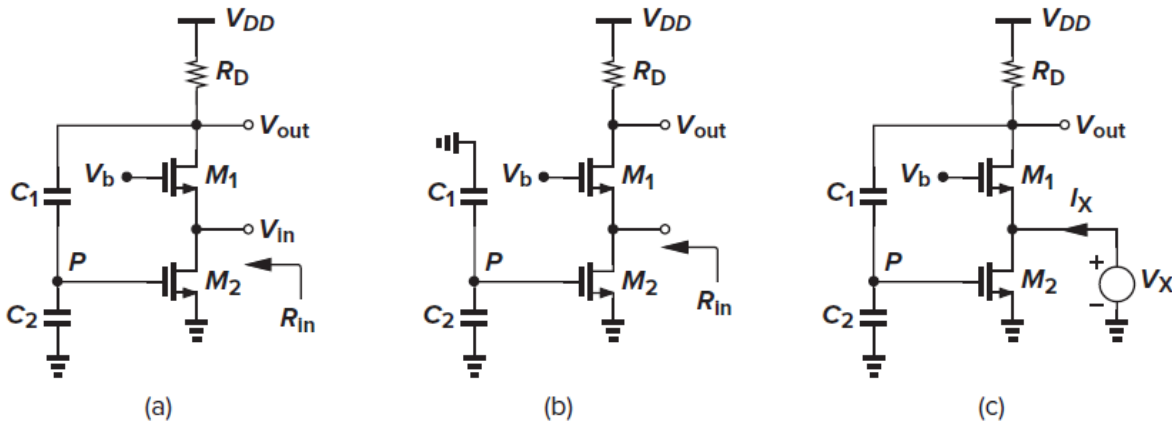


Figure 8.8 (a) Common-gate circuit with feedback; (b) open-loop circuit; (c) calculation of input resistance.

Bandwidth Modification. The next example illustrates the effect of negative feedback on the bandwidth. Suppose the feedforward amplifier has a one-pole transfer function:

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_0}} \quad (8.18)$$

where A_0 denotes the low-frequency gain and ω_0 is the 3-dB bandwidth. What is the transfer function of the closed-loop system? From (8.5), we have

$$\frac{Y}{X}(s) = \frac{\frac{A_0}{1 + \frac{s}{\omega_0}}}{1 + \beta \frac{A_0}{1 + \frac{s}{\omega_0}}} \quad (8.19)$$

$$= \frac{A_0}{1 + \beta A_0 + \frac{s}{\omega_0}} \quad (8.20)$$

$$= \frac{\frac{A_0}{1 + \beta A_0}}{1 + \frac{s}{(1 + \beta A_0)\omega_0}} \quad (8.21)$$

The numerator of (8.21) is simply the closed-loop gain at low frequencies—as predicted by (8.5)—and the denominator reveals a pole at $(1 + \beta A_0)\omega_0$. Thus, the 3-dB bandwidth has increased by a factor of $1 + \beta A_0$, albeit at the cost of a proportional reduction in the gain (Fig. 8.10).

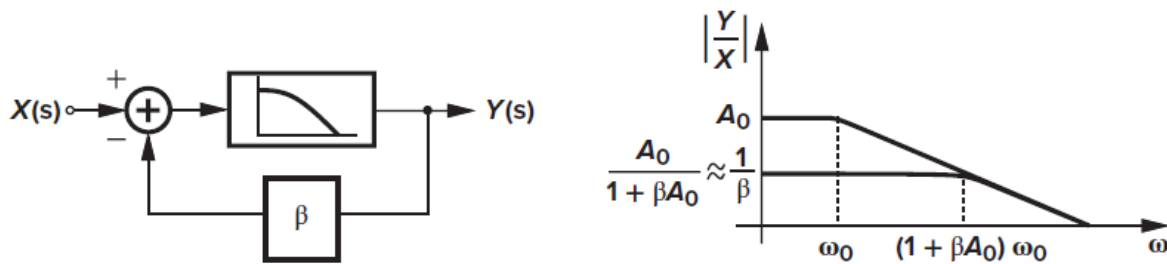


Figure 8.10 Bandwidth modification as a result of feedback.

The increase in the bandwidth fundamentally originates from the gain desensitization property of feedback. Recall from (8.6) that, if A is large enough, the closed-loop gain remains approximately equal to $1/\beta$ even if A experiences substantial variations. In the example of Fig. 8.10, A varies with frequency rather than process or temperature, but negative feedback still suppresses the effect of this variation. Of course, at high frequencies, A drops to such low levels that βA becomes comparable with unity and the closed-loop gain falls below $1/\beta$.

Nonlinearity Reduction

An important property of negative feedback is the reduction of nonlinearity in analog circuits. A nonlinear characteristic is one that departs from a straight line, i.e., one whose *slope* varies (Fig. 8.12). A familiar example is the input-output characteristic of differential pairs. Note that

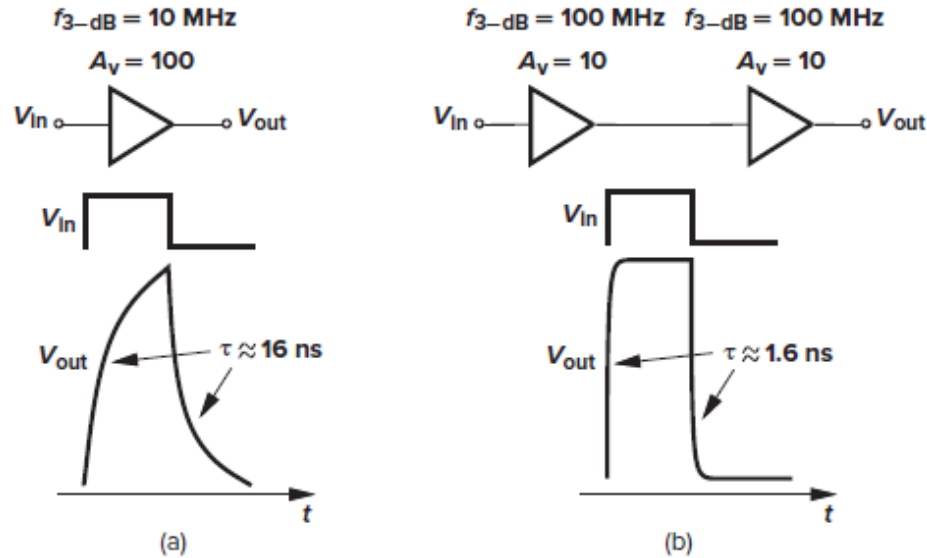


Figure 8.11 Amplification of a 20-MHz square wave by (a) a 10-MHz amplifier and (b) a cascade of two 100-MHz feedback amplifiers.

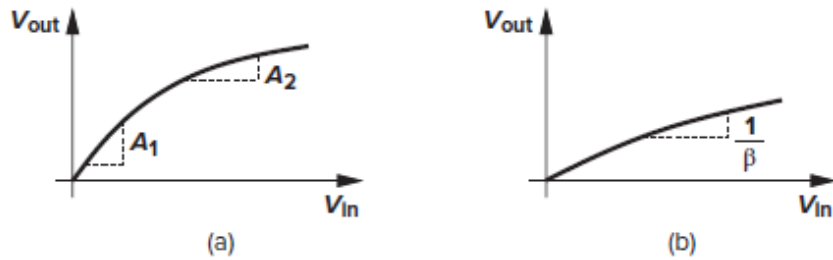


Figure 8.12 Input-output characteristic of a nonlinear amplifier (a) before and (b) after applying feedback.

the slope can be viewed as the small-signal gain. We predict that, even though the gain of an open-loop amplifier varies from A_1 to A_2 in Fig. 8.12, a closed-loop feedback system incorporating such an amplifier exhibits less gain variation and hence a higher linearity. To quantify this effect, we note that the open-loop gain ratio between regions 1 and 2 in Fig. 8.12 is equal to

$$r_{open} = \frac{A_2}{A_1} \quad (8.22)$$

For example, $r_{open} = 0.9$ means that the gain falls by 10% from region 1 to region 2. Assuming $A_2 = A_1 - \Delta A$, we can write

$$r_{open} = 1 - \frac{\Delta A}{A_1} \quad (8.23)$$

Let us place this amplifier in a negative-feedback loop. For the closed-loop gain ratio, we have

$$r_{closed} = \frac{\frac{A_2}{1 + \beta A_2}}{\frac{A_1}{1 + \beta A_1}} \quad (8.24)$$

$$= \frac{1 + \frac{1}{\beta A_1}}{1 + \frac{1}{\beta A_2}} \quad (8.25)$$

It follows that

$$r_{closed} \approx 1 - \frac{\frac{1}{\beta A_2} - \frac{1}{\beta A_1}}{1 + \frac{1}{\beta A_2}} \quad (8.26)$$

$$\approx 1 - \frac{A_1 - A_2}{1 + \beta A_2} \frac{1}{A_1} \quad (8.27)$$

$$\approx 1 - \frac{\Delta A}{1 + \beta A_2} \frac{1}{A_1} \quad (8.28)$$

Comparison of (8.23) and (8.28) suggests that the gain ratio is much closer to 1 in the latter if the loop gain, $1 + \beta A_2$, is large.

2. Types of Negative feedback amplifier

Voltage – voltage feedback amplifier

This topology senses the output voltage and returns the feedback signal as a voltage.⁷ Following the conceptual illustrations of Figs. 8.17 and 8.18, we note that the feedback network is connected in *parallel* with the output and in *series* with the input port (Fig. 8.21). An ideal feedback network in this case exhibits infinite input impedance and zero output impedance because it senses a voltage and generates a voltage. We can therefore write $V_F = \beta V_{out}$, $V_e = V_{in} - V_F$, $V_{out} = A_0(V_{in} - \beta V_{out})$, and hence

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \beta A_0} \quad (8.31)$$

We recognize that βA_0 is the loop gain and that the overall gain has dropped by $1 + \beta A_0$. Note that here both A_0 and β are dimensionless quantities.

As a simple example of voltage-voltage feedback, suppose we employ a differential voltage amplifier with single-ended output as the feedforward amplifier and a resistive divider as the feedback network

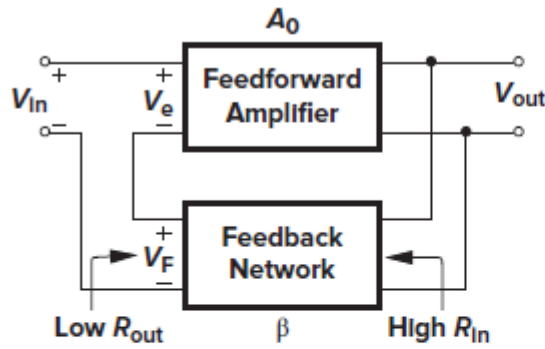


Figure 8.21 Voltage-voltage feedback.

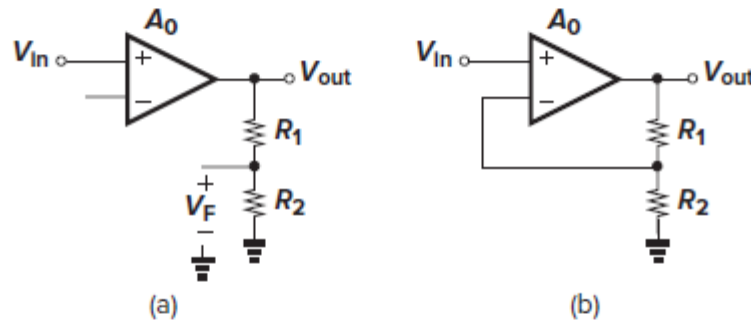


Figure 8.22 (a) Amplifier with output sensed by a resistive divider; (b) voltage-voltage feedback amplifier.

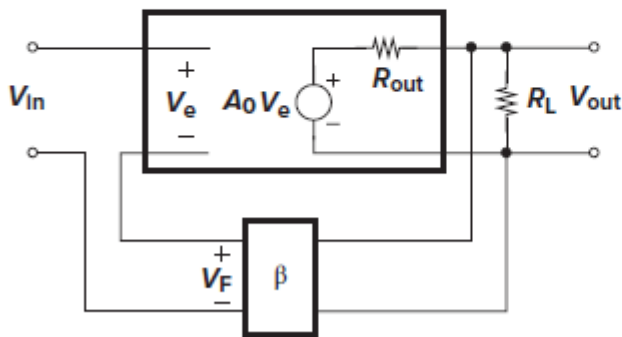


Figure 8.23 Effect of voltage-voltage feedback on output resistance.

The divider senses the output voltage, producing a fraction thereof as the feedback signal V_F . Following the block diagram of Fig. 8.21, we place V_F in series with the input of the amplifier to perform subtraction of voltages [Fig. 8.22(b)].

How does voltage-voltage feedback modify the input and output impedances? Let us first consider the output impedance. Recall that a negative-feedback system attempts to make the output an accurate (scaled) replica of the input. Now suppose, as shown in Fig. 8.23, we load the output by a resistor R_L , gradually decreasing its value. While in the open-loop configuration, the output would simply drop in proportion to $R_L/(R_L + R_{out})$, in the feedback system, V_{out} is maintained as a reasonable replica of V_{in} even though R_L decreases. That is, so long as the loop gain remains much greater than unity, $V_{out}/V_{in} \approx 1/\beta$, regardless of the value of R_L .

From another point of view, since the circuit stabilizes (“regulates”) the output voltage amplitude despite load variations, it behaves as a *voltage* source, thus exhibiting a low output impedance. This property fundamentally originates from the gain desensitization provided by feedback.

In order to formally prove that voltage feedback lowers the output impedance, we consider the simple model in Fig. 8.24, where R_{out} represents the output impedance of the feedforward amplifier. Setting the input to zero and applying a voltage at the output, we write $V_F = \beta V_X$, $V_e = -\beta V_X$, $V_M = -\beta A_0 V_X$,

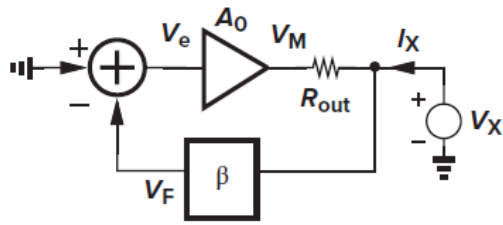


Figure 8.24 Calculation of output resistance of a voltage-voltage feedback circuit.

and hence $I_X = [V_X - (-\beta A_0 V_X)]/R_{out}$ (if the current drawn by the feedback network is neglected). It follows that

$$\frac{V_X}{I_X} = \frac{R_{out}}{1 + \beta A_0} \quad (8.32)$$

Thus, the output impedance and the gain are lowered by the same factor. In the circuit of Fig. 8.22(b), for example, the output impedance is lowered by $1 + A_0 R_2/(R_1 + R_2)$.

Current-Voltage Feedback

In some circuits, it is desirable or simpler to sense the output current to perform feedback. The current is actually sensed by placing a (preferably small) resistor in series with the output and using the voltage drop across the resistor as the feedback information. This voltage may even serve as the return signal that is directly subtracted from the input.

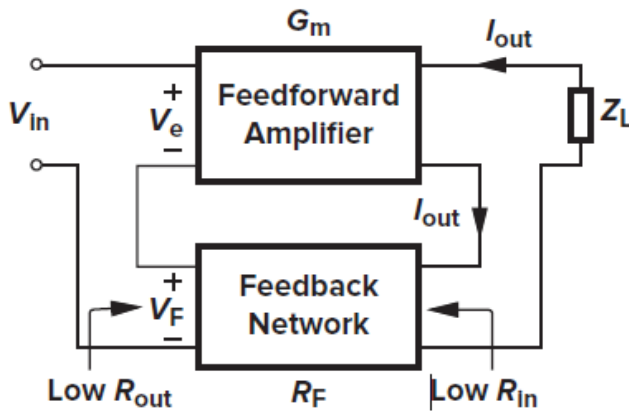


Figure 8.30 Current-voltage feedback.

Let us consider the general current-voltage feedback system illustrated in Fig. 8.30. Since the feedback network senses the output current and returns a voltage, its feedback factor, β , has the dimension of resistance and is denoted by R_F . It is important to note that a G_m stage must be loaded (“terminated”) by a finite impedance, Z_L , to ensure that it can deliver its output current. If $Z_L = \infty$, then an ideal G_m stage would sustain an infinite output voltage. We write $V_F = R_F I_{out}$, $V_e = V_{in} - R_F I_{out}$, and hence $I_{out} = G_m(V_{in} - R_F I_{out})$. It follows that

$$\frac{I_{out}}{V_{in}} = \frac{G_m}{1 + G_m R_F}$$

An ideal feedback network in this case exhibits zero input and output impedances.

It is instructive to confirm that $G_m R_F$ is indeed the loop gain. As shown in Fig. 8.31, we set the input voltage to zero and break the loop by disconnecting the feedback network from the output and replacing it with a *short* at the output (if the feedback network is ideal). We then inject the test signal I_t , producing $V_F = R_F I_t$, and hence $I_{out} = -G_m R_F I_t$. Thus, the loop gain is equal to $G_m R_F$ and the transconductance of the amplifier is reduced by $1 + G_m R_F$ when feedback is applied.

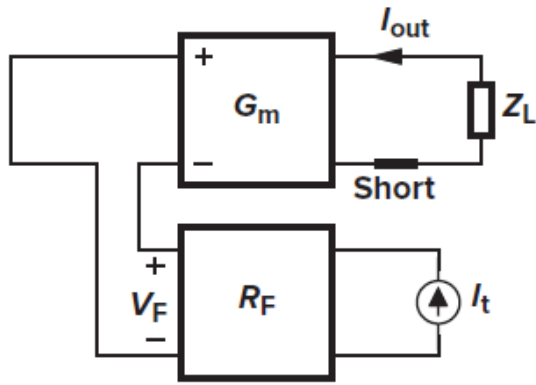


Figure 8.31 Calculation of loop gain for current-voltage feedback.

Is it realistic to assume that the input impedance of the feedback network is zero? Why do we use a test current rather than a test voltage? Does the type of test source affect the loop gain calculations? These questions are addressed later in this chapter.

Sensing the current at the output of a feedback system *increases* the output impedance. This is because the system attempts to make the output *current* a faithful replica of the input signal (with a proportionality factor if the input is a voltage quantity). Consequently, the system delivers the same current waveform as the load varies, in essence approaching an ideal current source and hence exhibiting a high output impedance.

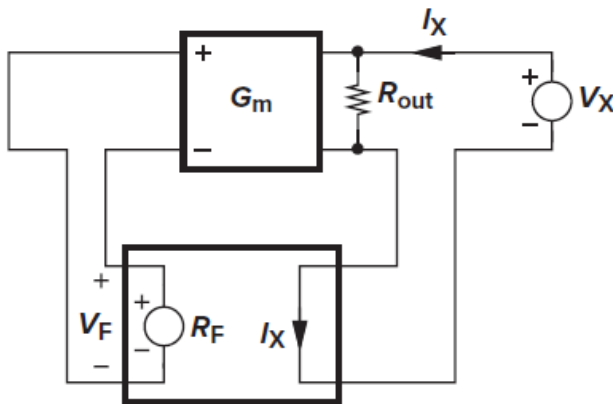


Figure 8.32 Calculation of output resistance of a current-voltage feedback amplifier.

To prove the above result, we consider the current-voltage feedback topology shown in Fig. 8.32, where R_{out} represents the finite output impedance of the feedforward amplifier.¹⁰ The feedback network produces a voltage V_F proportional to I_X : $V_F = R_F I_X$, and the current generated by G_m equals $-R_F I_X G_m$. As a result, $-R_F I_X G_m = I_X - V_X/R_{out}$, yielding

$$\frac{V_X}{I_X} = R_{out}(1 + G_m R_F) \quad (8.41)$$

The output impedance therefore increases by a factor of $1 + G_m R_F$.

Voltage-Current Feedback

In this type of feedback, the output voltage is sensed and a proportional current is returned to the summing point at the input.¹¹ Note that the feedforward path incorporates a transimpedance amplifier with gain R_0 and the feedback factor has a dimension of conductance.

A voltage-current feedback topology is shown in Fig. 8.35. Sensing a voltage and producing a current, the feedback network is characterized by a transconductance g_{mF} , ideally exhibiting infinite input and output impedances. Since $I_F = g_{mF} V_{out}$ and $I_e = I_{in} - I_F$, we have $V_{out} = R_0 I_e = R_0(I_{in} - g_{mF} V_{out})$.

It follows that

$$\frac{V_{out}}{I_{in}} = \frac{R_0}{1 + g_{mF} R_0} \quad (8.45)$$

The reader can prove that $g_{mF} R_0$ is indeed the loop gain, concluding that this type of feedback lowers the transimpedance by a factor equal to one plus the loop gain.

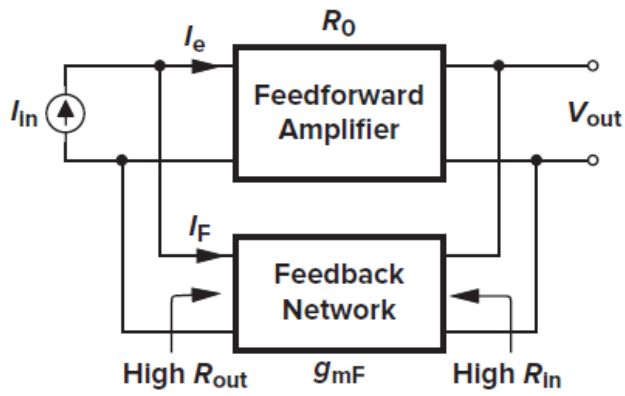


Figure 8.35 Voltage-current feedback.

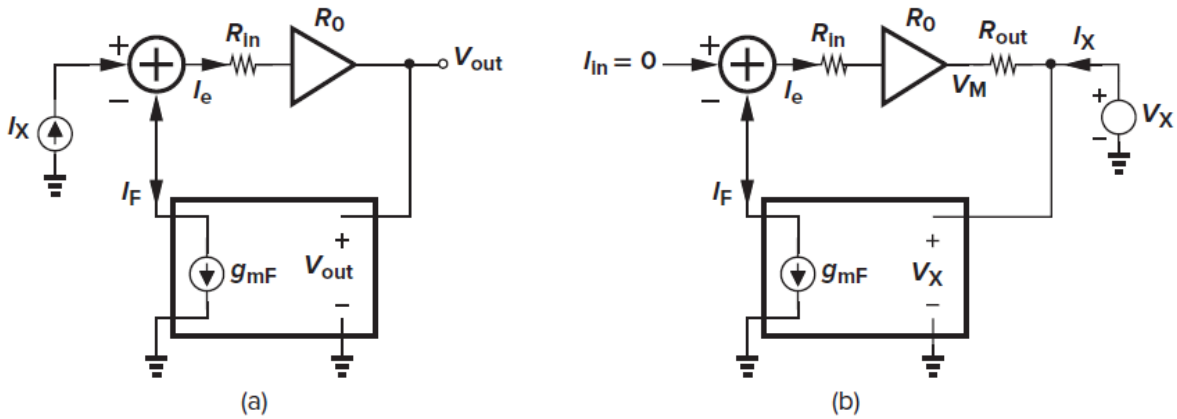


Figure 8.38 Calculation of (a) input and (b) output impedance of a voltage-current feedback amplifier.

Current-Current Feedback

Figure 8.41 illustrates this type of feedback.¹² Here, the feedforward amplifier is characterized by a current gain, A_I , and the feedback network by a current ratio, β . In a fashion similar to the previous derivations, the reader can easily prove that the closed-loop current gain is equal to $A_I/(1 + \beta A_I)$, the input impedance is divided by $1 + \beta A_I$ and the output impedance is multiplied by $1 + \beta A_I$.

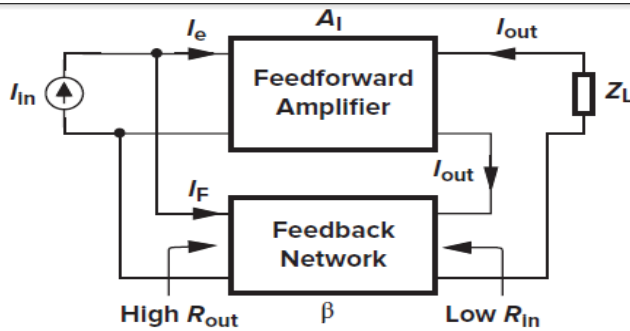


Figure 8.41 Current-current feedback.

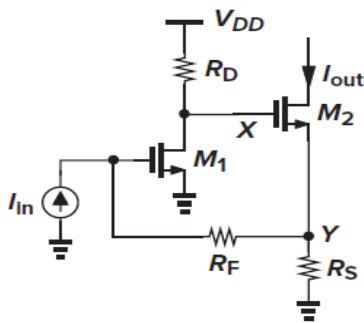


Figure 8.42

Figure 8.42 illustrates an example of current-current feedback. Here, since the source and drain currents of M_2 are equal (at low frequencies), resistor R_S is inserted in the source network to monitor the output current. Resistor R_F plays the same role as in Fig. 8.39.

3. Effect of loading in feedback networks.

The analysis is carried out in three steps:

- (1) open the loop with proper loading and calculate the open-loop gain, A_{OL} , and the open-loop input and output impedances;
- (2) determine the feedback ratio, β , and hence the loop gain, βA_{OL} ; and
- (3) calculate the closed-loop gain and input and output impedances by scaling the open-loop values by a factor of $1 + \beta A_{OL}$.

Note that in the equations defining β , the subscripts 1 and 2 refer to the input and output ports of the feedback network, respectively.

In this chapter, we have described two methods of obtaining the loop gain: (1) by breaking the loop at an arbitrary point, as shown in Fig. 8.5, and (2) by calculating A_{OL} and β , as illustrated in Fig. 8.67.

The two methods may yield slightly different results due to the issues outlined.

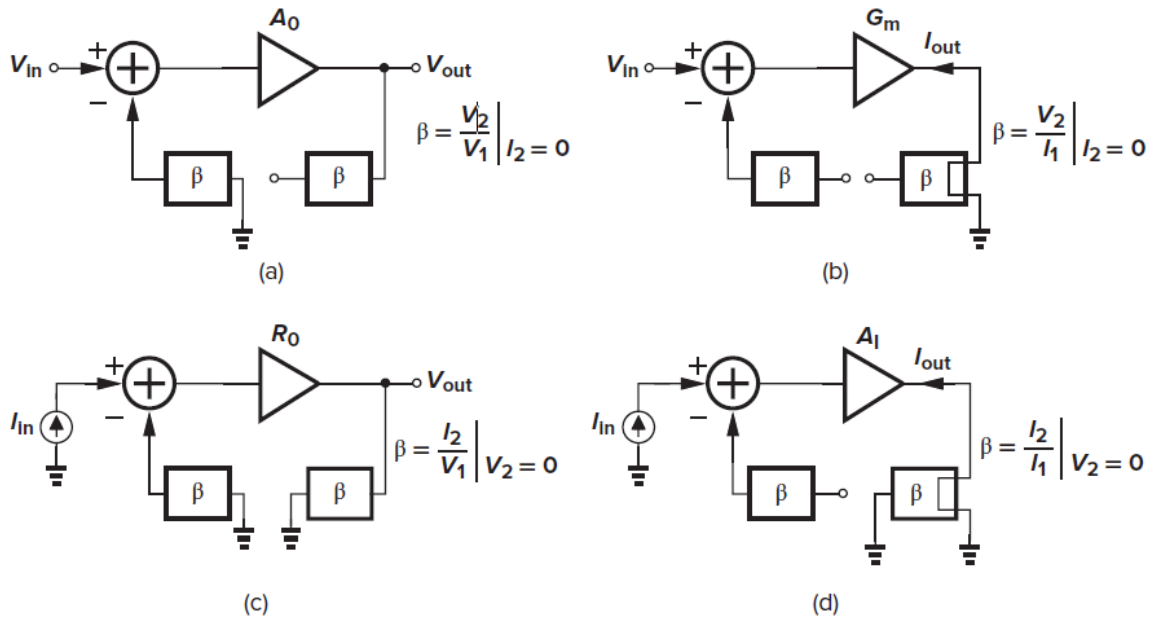


Figure 8.67 Summary of loading effects.

4. Performance Parameters

In this section, we describe a number of op amp design parameters, providing an understanding of why and where each may become important. For this discussion, we consider the differential cascode circuit

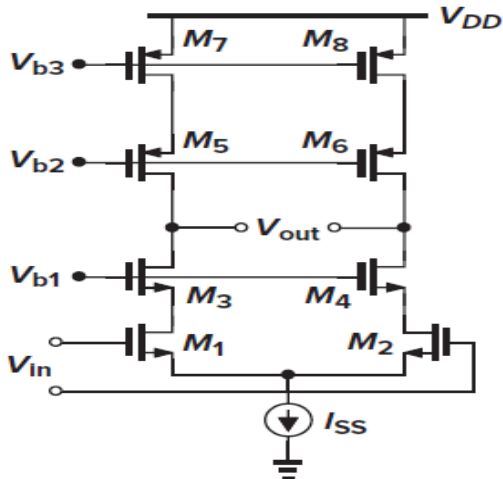


Figure 9.1 Cascode op amp.

shown in Fig. 9.1 as a representative op amp design.¹ The voltages $V_{b1} - V_{b3}$ are generated by the current mirror techniques described in Chapter 5.

Gain The open-loop gain of an op amp determines the precision of the feedback system employing the op amp. As mentioned before, the required gain may vary by four orders of magnitude according to the application. Trading with such parameters as speed and output voltage swings, the minimum required gain must therefore be known. As explained in Chapter 14, a high open-loop gain may also be necessary to suppress nonlinearity.

Small-Signal Bandwidth The high-frequency behavior of op amps plays a critical role in many applications. For example, as the frequency of operation increases, the open-loop gain begins to drop (Fig. 9.4), creating larger errors in the feedback system. The small-signal bandwidth is usually defined as the “unitygain” frequency, f_u , which can reach several gigahertz in today’s CMOS op amps. The 3-dB frequency, $f_{3\text{-dB}}$, may also be specified to allow easier prediction of the closed-loop frequency response.

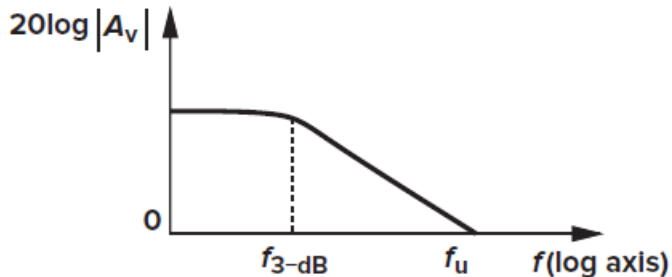


Figure 9.4 Gain roll-off with frequency.

Large-Signal Behavior In many of today’s applications, op amps must operate with large transient signals. Under these conditions, nonlinear phenomena make it difficult to characterize the speed merely by small-signal properties such as the open-loop response shown in Fig. 9.4. As an example, suppose the feedback circuit of Fig. 9.5 incorporates a realistic op amp (i.e., with finite output impedance) while driving a large load capacitance. How does the circuit behave if we apply a 1-V step at the input? Since the output voltage cannot change instantaneously, the voltage difference sensed by the op amp itself at $t \geq 0$ is equal to 1 V. Such a large difference momentarily drives the op amp into a nonlinear region of operation. (Otherwise, with an open-loop gain of, say, 1000, the op amp would produce 1000 V at the output.)

As explained in Sec. 9.9, the large-signal behavior is usually quite complex, calling for careful simulations.

Output Swing Most systems employing op amps require large voltage swings to accommodate a wide range of signal amplitudes. For example, a high-quality microphone that senses the music produced by an orchestra may generate instantaneous voltages that vary by more than four orders of magnitude, demanding that subsequent amplifiers and filters handle large swings (and/or achieve a low noise). The need for large output swings has made fully differential op amps popular. Similar to the circuits described in Chapter 4, such op amps generate “complementary” outputs, roughly doubling the available swing. Nonetheless, as mentioned in Chapters 3 and 4 and explained later in this chapter, the maximum voltage swing trades with device size and bias currents and hence speed. Achieving large swings is the principal challenge in today’s op amp design.

Linearity Open-loop op amps suffer from substantial nonlinearity. In the circuit of Fig. 9.1, for example, the input pair M_1 – M_2 exhibits a nonlinear relationship between its differential drain current and its input voltage. As explained in Chapter 14, the issue of nonlinearity is tackled by two approaches: using fully differential implementations to suppress even-order harmonics and allowing sufficient open-loop gain for the closed-loop feedback system to achieve adequate linearity. It is interesting to note that in many feedback circuits, the linearity requirement, rather than the gain error requirement, governs the choice of the open-loop gain.

Noise and Offset The input noise and offset of op amps determine the minimum signal level that can be processed with reasonable quality. In a typical op amp topology, several devices contribute noise and offset, necessitating large dimensions or bias currents. For example, in the circuit of Fig. 9.1, M_1 – M_2 and M_7 – M_8 contribute the most.

We should also recognize a trade-off between noise and *output swing*. For a given bias current, as the overdrive voltage of M_7 and M_8 in Fig. 9.1 is lowered to allow larger swings at the output, their transconductance increases and so does their drain noise current.

Supply Rejection Op amps are often employed in mixed-signal systems and sometimes connected to noisy digital supply lines. Thus, the performance of op amps in the presence of supply noise, especially as the noise frequency increases, is important. For this reason, fully differential topologies are preferred.

5. One stage operational amplifier

Basic Topologies

All of the differential amplifiers studied in Chapters 4 and 5 can be considered op amps. Figure 9.6 shows two such topologies with single-ended and differential outputs. The small-signal, low-frequency gain of both circuits is equal to $g_{mN}(r_{ON}r_{OP})$, where the subscripts N and P denote NMOS and PMOS, respectively. This value hardly exceeds 10 in nanometer technologies. The bandwidth is usually determined by the load capacitance, C_L . Note that the circuit of Fig. 9.6(a) exhibits a mirror pole (Chapter 6) whereas that of Fig. 9.6(b) does not, a critical difference in terms of the stability of feedback systems using these

topologies (Chapter 10).

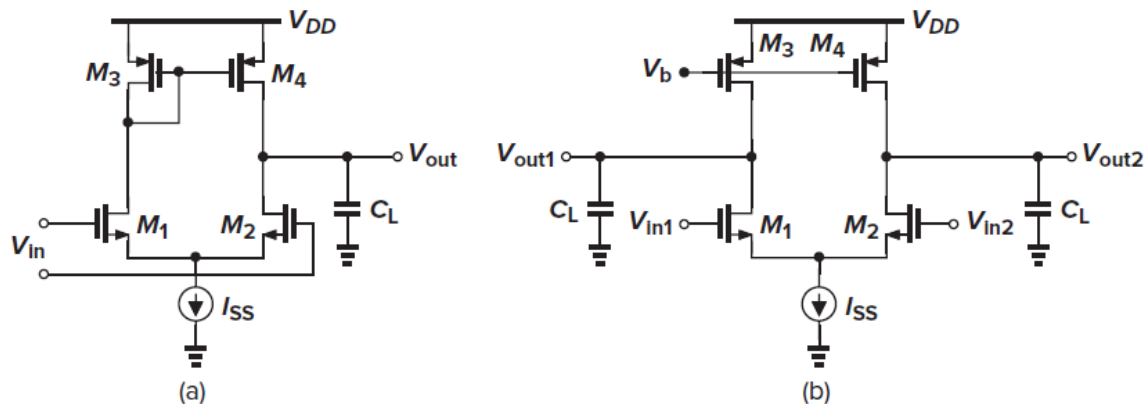


Figure 9.6 Simple op amp topologies.

The circuits of Fig. 9.6 suffer from noise contributions of M_1 – M_4 , as calculated in Chapter 7. Interestingly, in all op amp topologies, at least four devices contribute to the input noise: two input transistors and two “load” transistors.

In order to achieve a high gain, the differential cascode topologies of Chapters 4 and 5 can be used. Shown in Figs. 9.8(a) and (b) for single-ended and differential output generation, respectively, such circuits display a gain on the order of $g_m M[(g_m N F_{2ON})_{(g_m P F_{2OP})}]$, but at the cost of output swing and

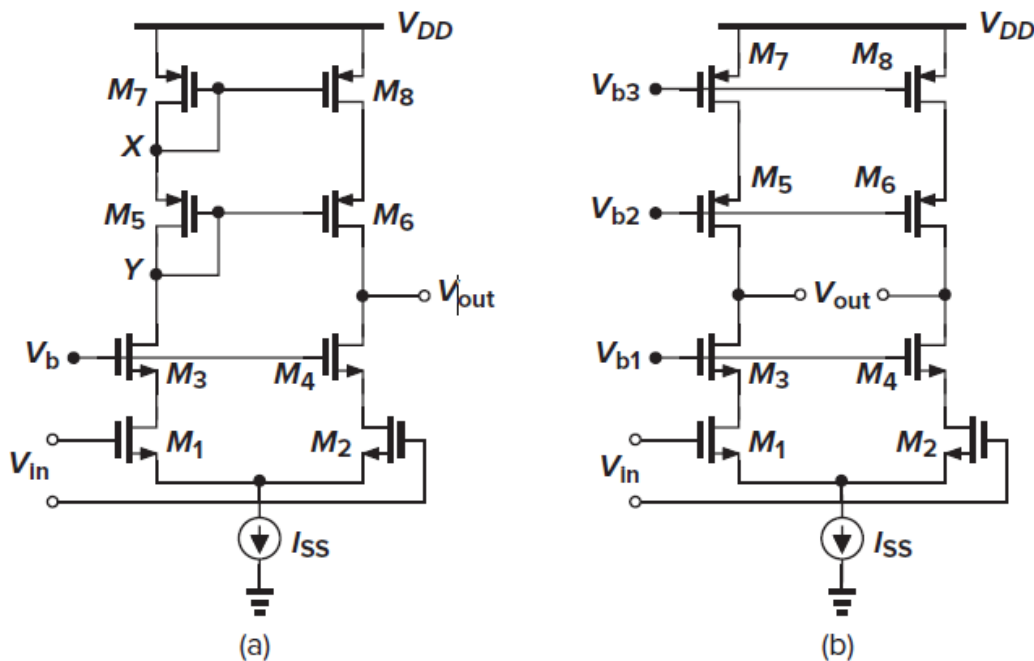


Figure 9.8 Cascode op amps.

additional poles. These configurations are also called “telescopic” cascode op amps to distinguish them from another cascode op amp described below. The circuit providing a single-ended output suffers from a mirror pole at node X (and a pole at Y), creating stability issues.

6. Two stage operational amplifier .

The op amps studied thus far exhibit a “one-stage” nature in that they allow the small-signal current produced by the input pair to flow directly through the output impedance, i.e., they perform voltage-to-current conversion only once. The gain of these topologies is therefore limited to the product of the input pair transconductance and the output impedance. We have also observed that cascoding in such circuits increases the gain while limiting the output swings.

In some applications, the gain and/or the output swings provided by cascode op amps are not adequate. For example, a modern amp must operate with supply voltages as low as 0.9 V while delivering single-ended output swings as large as 0.8 V. In such cases, we resort to “two-stage” op amps, with the first stage providing a high gain and the second, large swings (Fig. 9.22). In contrast to cascode op amps, a two-stage configuration isolates the gain and swing requirements.

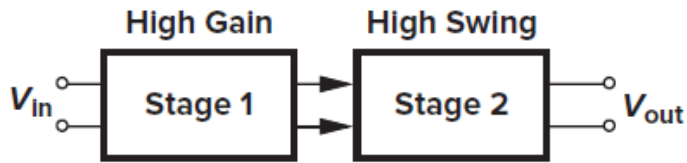


Figure 9.22 Two-stage op amp.

Each stage in Fig. 9.22 can incorporate various amplifier topologies studied in previous sections, but the second stage is typically configured as a simple common-source stage so as to allow maximum output swings. Figure 9.23 shows an example, where the first and second stages exhibit gains equal to $g_{m1,2}(r_{O1,2}r_{O3,4})$ and $g_{m5,6}(r_{O5,6}r_{O7,8})$, respectively. The overall gain is therefore comparable to that

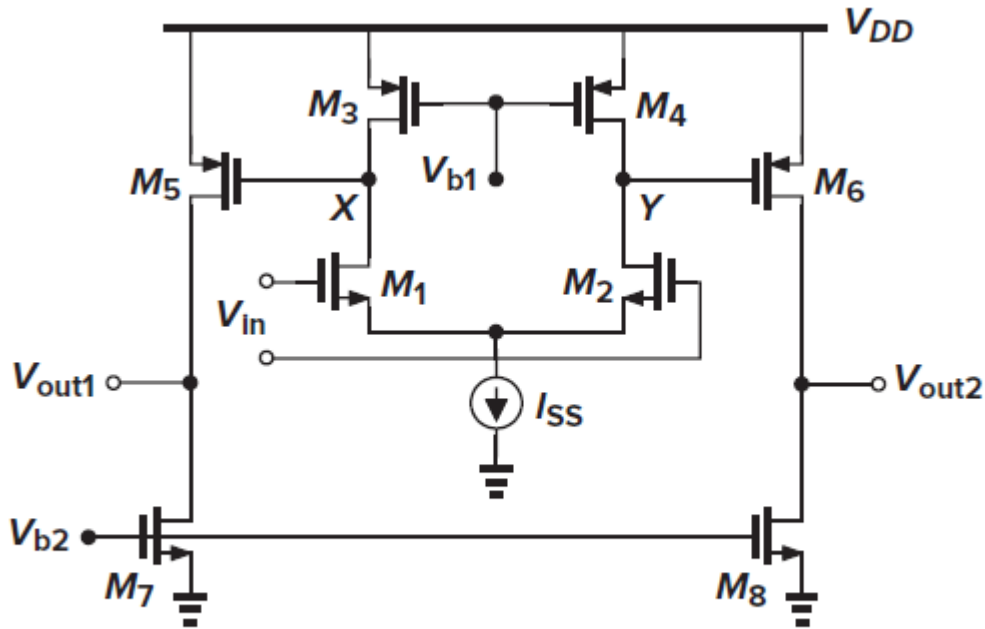


Figure 9.23 Simple implementation of a two-stage op amp.

of a cascode op amp, but the swing at V_{out1} and V_{out2} is equal to $V_{DD} - |V_{OD5,6}| - V_{OD7,8}$, the highest possible value.⁴

To obtain a higher gain, the first stage can incorporate cascode devices, as depicted in Fig. 9.24. With a gain of, say, 10 in the output stage, the voltage swings at X and Y are quite small, allowing optimization of M_1 – M_8 for higher gain. The overall voltage gain can be expressed as

$$A_v \approx \{g_{m1,2}[(g_{m3,4} + g_{mb3,4})r_{O3,4}r_{O1,2}]\|[(g_{m5,6} + g_{mb5,6})r_{O5,6}r_{O7,8}]\} \times [g_{m9,10}(r_{O9,10}\|r_{O11,12})] \quad (9.18)$$

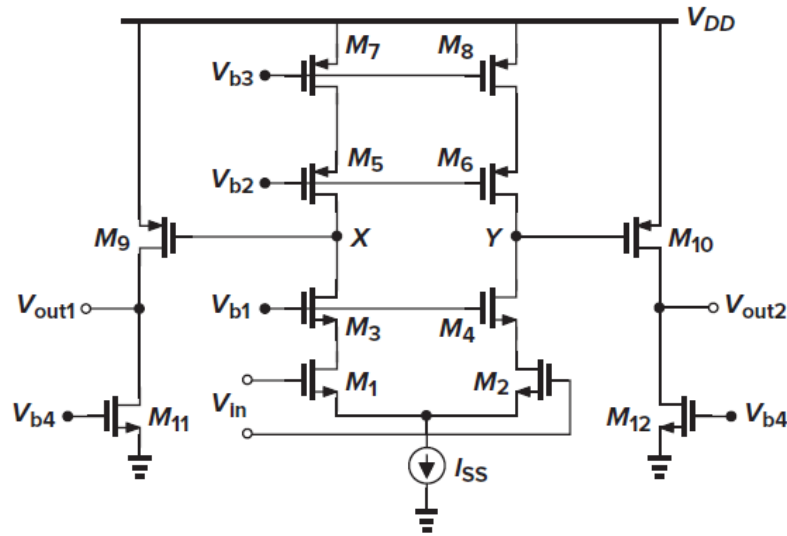


Figure 9.24 Two-stage op amp employing cascoding.

A two-stage op amp can provide a single-ended output. One method is to convert the differential currents of the two output stages to a single-ended voltage. Illustrated in Fig. 9.25, this approach maintains the differential nature of the first stage, using only the current mirror M_7 – M_8 to generate a single-ended output.

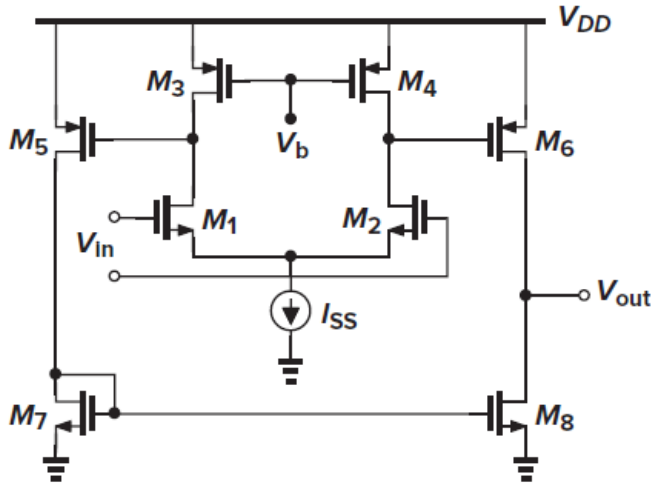


Figure 9.25 Two-stage op amp with single-ended output.

7. Gain boosting

The limited gain of the one-stage op amps studied in Sec. 9.2 and the difficulties in using two-stage op amps at high speeds have motivated extensive work on new topologies. Recall that in one-stage op amps, such as telescopic and folded-cascode topologies, the objective is to maximize the output impedance so as to attain a high voltage gain. The idea behind gain boosting is to further increase the output impedance without adding more cascode devices [4, 5]. We neglect body effect for simplicity, but it can be readily included at the end.

First Perspective Suppose a transistor is preceded by an ideal voltage amplifier as shown in Fig. 9.26(a).

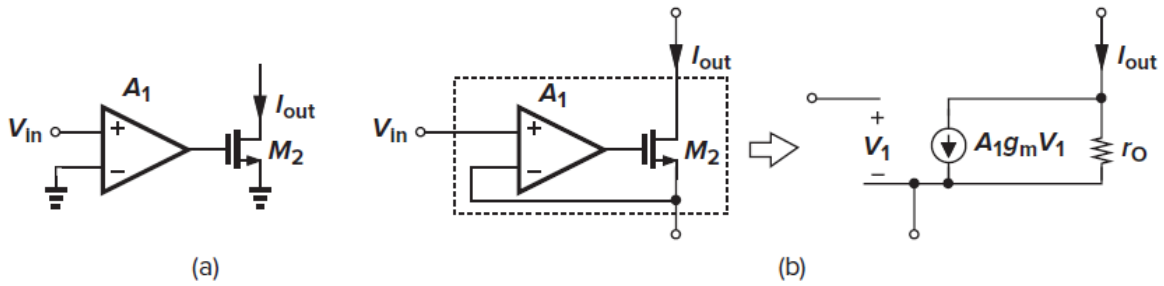


Figure 9.26 (a) Transistor preceded by a voltage amplifier, and (b) equivalent circuit.

We note that the overall circuit exhibits a transconductance of $A_1 g_m$ and a voltage gain of $-A_1 g_m r_O$ (why?). We thus surmise that this arrangement can be viewed as a three-terminal device (a “supertransistor”) having a transconductance of $A_1 g_m$ and an output resistance of r_O [Fig. 9.26(b)]. We neglect body effect in this section.

Let us now incorporate this new device in a familiar topology and examine the circuit’s behavior. We begin with the degenerated stage depicted in Fig. 9.27(a) and wish to compute its transconductance (with the output shorted to ac ground). Since R_S carries I_{out} , the small-signal gate voltage is given by $(V_{in} - R_S I_{out})A_1$, yielding a gate-source voltage of $(V_{in} - R_S I_{out})A_1 - R_S I_{out}$ and hence $I_{out} = g_m[(V_{in} - R_S I_{out})A_1 - R_S I_{out}]$. It follows that

$$\frac{I_{out}}{V_{in}} = \frac{A_1 g_m}{1 + (A_1 + 1)g_m R_S} \quad (9.19)$$

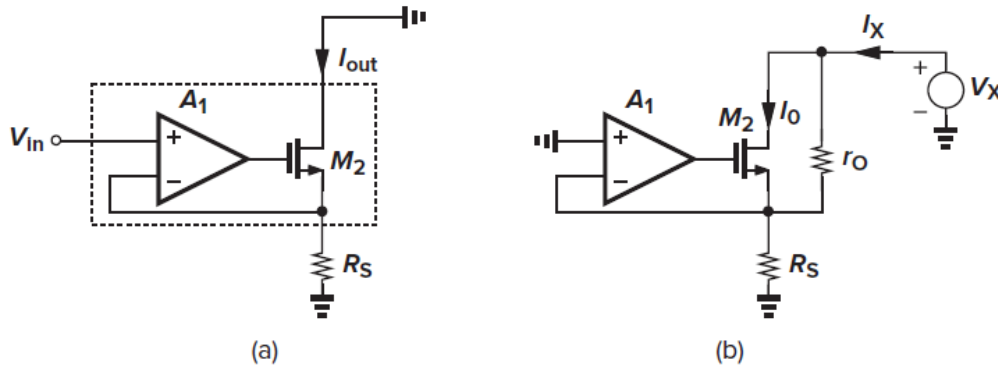


Figure 9.27 Arrangements for calculation of (a) transconductance, and (b) output resistance.

Without A_1 , the transconductance would be equal to $g_m/(1 + g_m R_S)$. Interestingly, the equivalent transconductance has risen by a factor of A_1 in the numerator and $A_1 + 1$ in the denominator, revealing that the model shown in Fig. 9.26(b) is not quite correct. However, since in practice $A_1 \gg 1$, the error introduced by this model is acceptably low.

How about the output resistance of the degenerated stage? From the setup in Fig. 9.27(b), we can express the voltage drop across R_S as $I_X R_S$ and the gate voltage of M_2 as $-A_1 I_X R_S$. That is, $I_O = (-A_1 R_S I_X - R_S I_X)g_m$. Also, r_O carries a current equal to $(V_X - R_S I_X)/r_O$. We now have

$$I_X = (-A_1 R_S - R_S)g_m I_X + \frac{V_X - R_S I_X}{r_O} \quad (9.20)$$

$$R_{out} = r_O + (A_1 + 1)g_m r_O R_S + R_S \quad (9.21)$$

Without A_1 , the output resistance would be equal to $r_O + g_m r_O R_S + R_S$.

Equation (9.21) is a remarkable result, suggesting that the output resistance of the circuit is “boosted,” as if the transconductance of M_2 were raised by a factor of $A_1 + 1$. This increase in R_{out} is afforded while the degenerated stage retains its voltage headroom. We can see that the allowable voltage swing at the

drain of M_2 is approximately the same for this structure and a simple degenerated transistor.

Circuit Implementation

In this section, we deal with the implementation of the auxiliary amplifier in the regulated cascode and extend the gain-boosting technique to op amps. The simplest realization of A_1 is a common-source stage, as shown in Fig. 9.32(a). If I_1 is ideal, then $|A_1| = g_{m3}r_{O3}$, yielding $|V_{out}/V_{in}| \approx g_{m1}r_{O1}g_{m2}r_{O2}(g_{m3}r_{O3} + 1)$, as in a *triple* cascode. However, this topology limits the output voltage swing because the minimum voltage at node P is dictated by V_{GS3} rather than the overdrive of M_1 . We note that V_{out} must remain above $V_{GS3} + (V_{GS2} - V_{TH2})$ here.

Frequency Response

Recall that the premise behind gain boosting is to increase the gain without adding a second stage or more cascode devices. Does this mean that the op amps of Fig. 9.36 have a one-stage nature? After all, the gain-boosting amplifier introduces its own pole(s). In contrast to two-stage op amps, where the entire signal experiences the poles associated with each stage, in a gain-boosted op amp, most of the signal flows directly through the cascode devices to the output. Only a small “error” component is processed by the auxiliary amplifier and “slowed down.”

In order to analyze the frequency response of the regulated cascode, we simplify the circuit to that shown in Fig. 9.37, where the auxiliary amplifier contains one pole at ω_0 , $A_1(s) = A_0/(1 + s/\omega_0)$, and only the load capacitance, C_L , is included. We wish to determine $V_{out}/V_{in} = -G_m Z_{out}$. To compute $G_m(s)$ (with the output node grounded), we note from Example 9.11 that the impedance seen looking into the source of M_2 is equal to $r_{O2}[1 + (A_1 + 1)g_{m2}r_{O2}]$, and divide the drain current of M_1 between this impedance and r_{O1} :

8. Input Range Limitation

The op amp circuits studied thus far have evolved to achieve large differential output swings. While the differential input swings are usually much smaller (by a factor equal to the open-loop gain), the input *common-mode* level may need to vary over a wide range in some applications. For example, consider the simple unity-gain buffer shown in Fig. 9.65, where the input swing is nearly equal to the output swing. Interestingly, in this case the voltage swings are limited by the input differential pair rather than the output

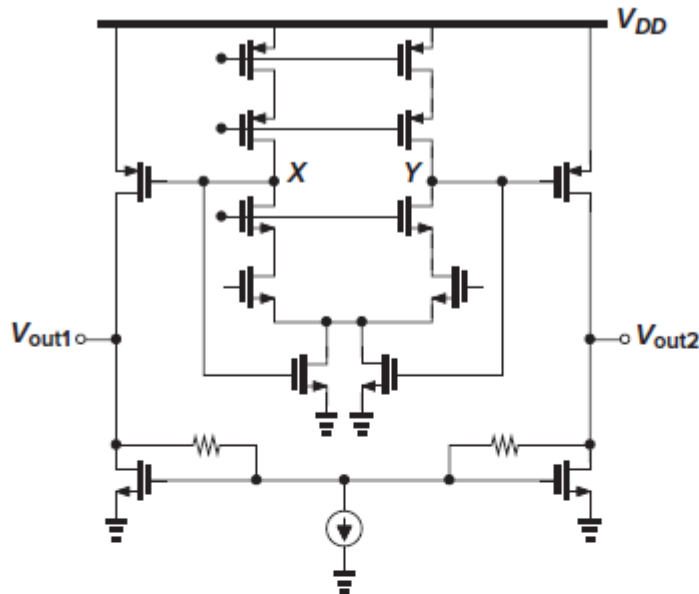


Figure 9.64 CMFB loops around cascode and output stages.

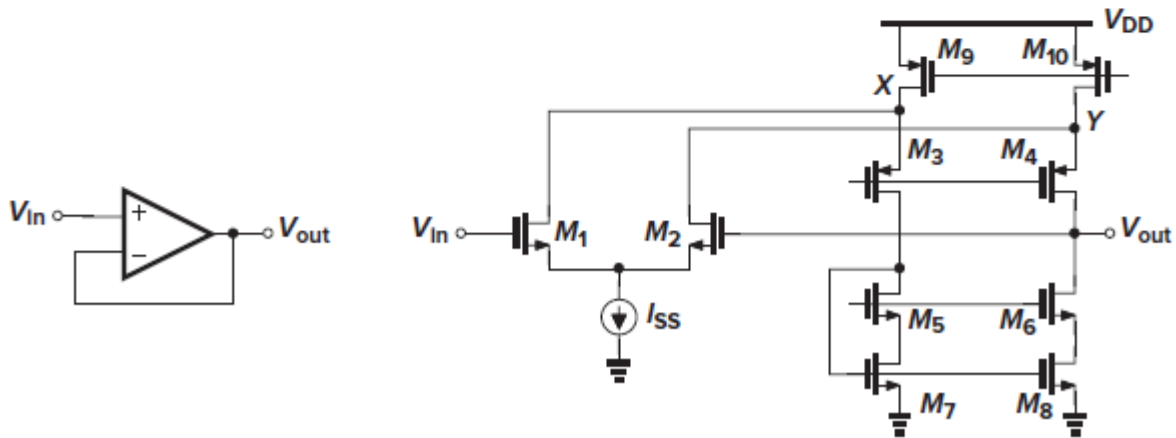


Figure 9.65 Unity-gain buffer.

cascode branch. Specifically, $V_{in,min} \approx V_{out,min} = V_{GS1,2} + V_{ISS}$, approximately one threshold voltage higher than the allowable minimum provided by M_5 – M_8 .

What happens if V_{in} falls below the minimum given above? The MOS transistor operating as I_{SS} enters the triode region, decreasing the bias current of the differential pair and hence lowering the transconductance. We then postulate that the limitation is overcome if the transconductance can somehow be restored.

A simple approach to extending the input CM range is to incorporate both NMOS and PMOS differential pairs such that when one is “dead,” the other is “alive.” Illustrated in Fig. 9.66, the idea is to combine two folded-cascode op amps with NMOS and PMOS input differential pairs. Here, as the input CM level approaches the ground potential, the NMOS pair’s transconductance drops, eventually falling to zero. Nonetheless, the PMOS pair remains active, allowing normal operation. Conversely, if the input CM level approaches V_{DD} , M_{1P} and M_{2P} begin to turn off, but M_1 and M_2 function properly.

An important concern in the circuit of Fig. 9.66 is the variation of the overall transconductance of the two pairs as the input CM level changes. Considering the operation of each pair, we anticipate the behavior depicted in Fig. 9.67. Thus, many properties of the circuit, including gain, speed, and noise, vary.

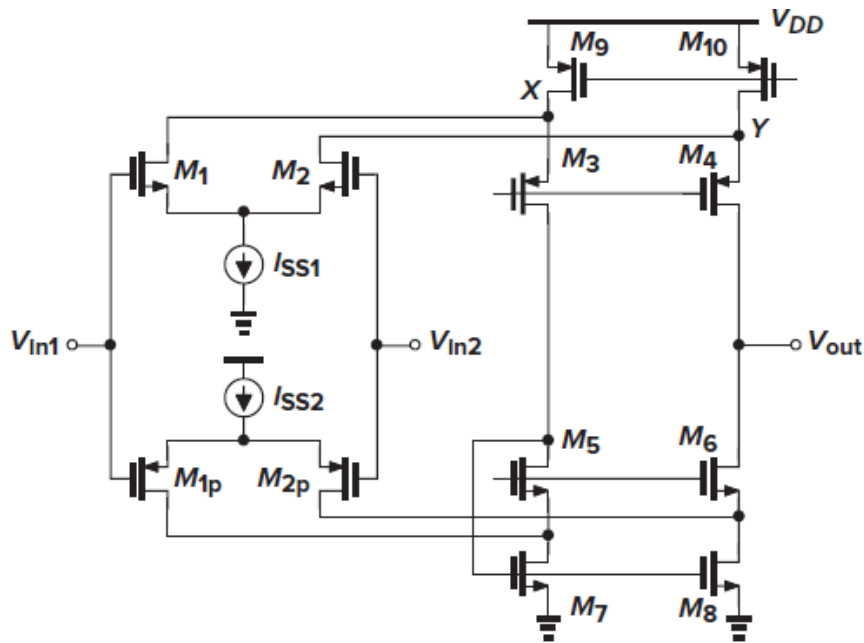


Figure 9.66 Extension of input CM range.

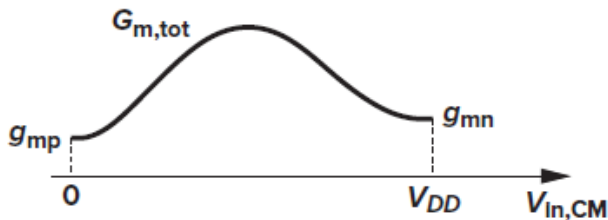


Figure 9.67 Variation of equivalent transconductance with the input CM level.

9.Slew Rate

Op amps used in feedback circuits exhibit a large-signal behavior called “slewing.” We first describe an interesting property of *linear* systems that vanishes during slewing. Consider the simple RC network shown in Fig. 9.68, where the input is an ideal voltage step of height V_0 . Since $V_{out} = V_0[1 - \exp(-t/\tau)]$, where $\tau = RC$, we have

$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau} \exp \frac{-t}{\tau} \quad (9.58)$$

That is, the slope of the step response is proportional to the final value of the output; if we apply a larger input step, the output rises more rapidly. This is a fundamental property of linear systems: if the input amplitude is, say, doubled while other parameters remain constant, the output signal level must double at *every* point, leading to a twofold increase in the slope.

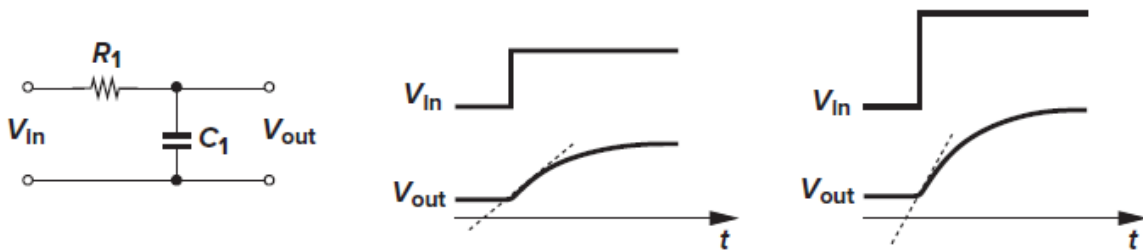


Figure 9.68 Response of a linear circuit to an input step.

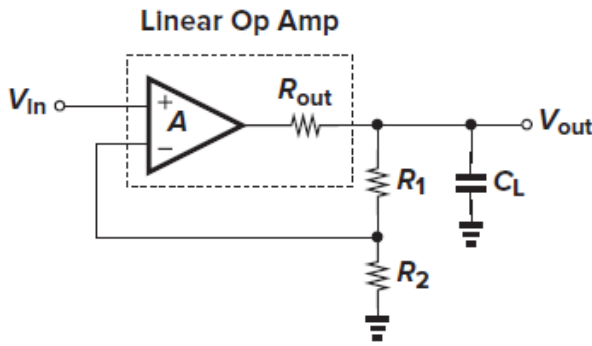


Figure 9.69 Response of linear op amp to step response.

The foregoing observation applies to linear feedback systems as well. Shown in Fig. 9.69 is an example, where the op amp is assumed linear. Here, we can write

$$\left[\left(V_{in} - V_{out} \frac{R_2}{R_1 + R_2} \right) A - V_{out} \right] \frac{1}{R_{out}} = \frac{V_{out}}{R_1 + R_2} + V_{out} C_L s \quad (9.59)$$

Assuming $R_1 + R_2 \gg R_{out}$, we have

$$\frac{V_{out}(s)}{V_{in}} \approx \frac{A}{\left(1 + A \frac{R_2}{R_1 + R_2} \right) \left[1 + \frac{R_{out} C_L}{1 + A R_2 / (R_1 + R_2)} s \right]} \quad (9.60)$$

As expected, both the low-frequency gain and the time constant are divided by $1 + A R_2 / (R_1 + R_2)$. The step response is therefore given by

$$V_{out} \approx V_0 \frac{A}{1 + A \frac{R_2}{R_1 + R_2}} \left[1 - \exp \frac{-t}{\frac{C_L R_{out}}{1 + A R_2 / (R_1 + R_2)}} \right] u(t) \quad (9.61)$$

indicating that the slope is proportional to the final value. This type of response is called “linear settling.” With a realistic op amp, on the other hand, the step response of the circuit begins to deviate from (9.61) as the input amplitude increases. Illustrated in Fig. 9.70, the response to sufficiently small inputs follows the exponential of Eq. (9.61), but with large input steps, the output displays a linear ramp having a constant slope. Under this condition, we say that the op amp experiences slewing and call the slope of the ramp the “slew rate.”

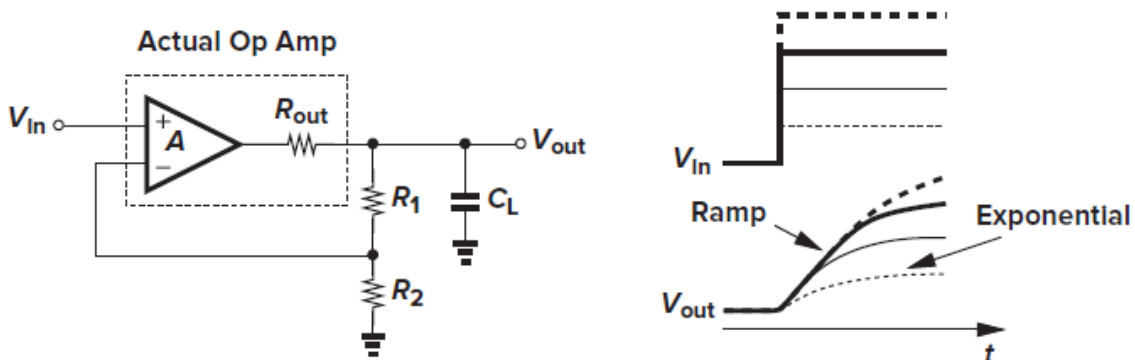


Figure 9.70 Slewing in an op amp circuit.

To understand the origin of slewing, let us replace the op amp of Fig. 9.70 by a simple CMOS implementation (Fig. 9.71), assuming for simplicity that $R_1 + R_2$ is very large. We first examine the circuit with a small input step. If V_{in} experiences a change of ΔV , I_{D1} increases by $g_{m1} \Delta V / 2$ and I_{D2} decreases by $g_{m1} \Delta V / 2$. Since the mirror action of M_3 and M_4 raises $|I_{D4}|$ by $g_{m1} \Delta V / 2$, the total smallsignal current provided by the op amp equals $g_{m1} \Delta V$. This current begins to charge C_L , but as V_{out} rises, so does V_X , reducing the difference between V_{G1} and V_{G2} and hence the output current of the op amp.

As a result, V_{out} varies according to (9.61).

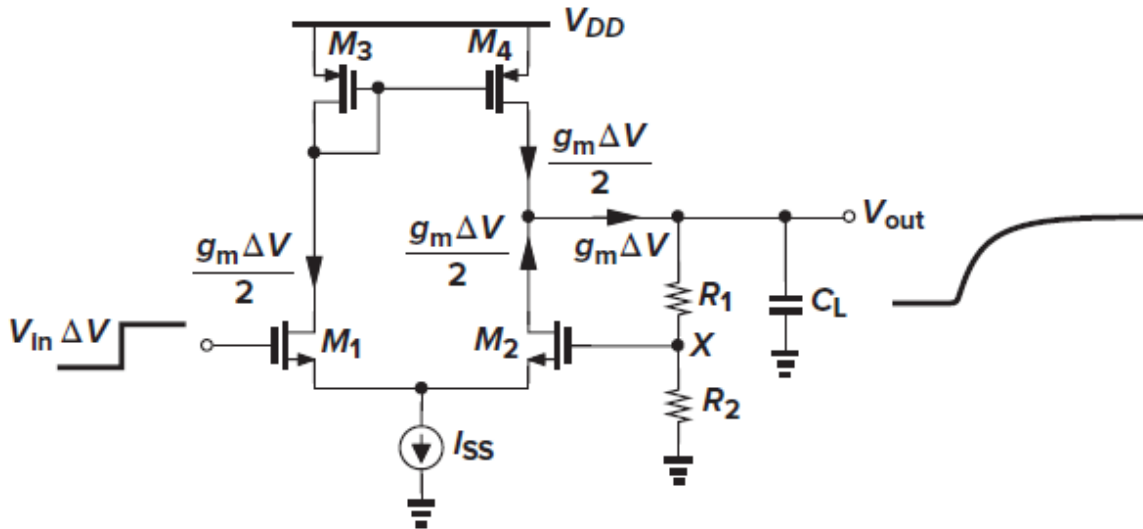
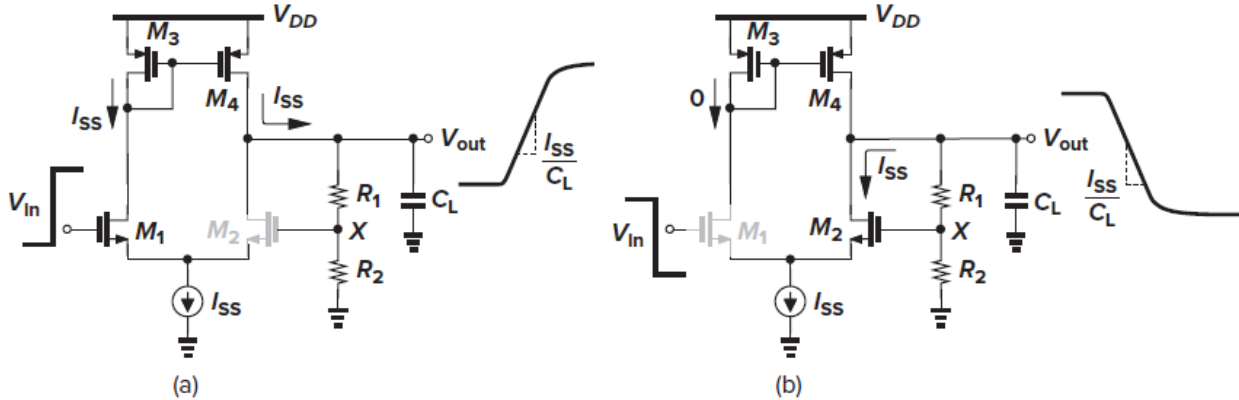


Figure 9.71 Small-signal operation of a simple op amp.

Now suppose V_{in} is so large that M_1 absorbs all of I_{SS} , turning off M_2 . The circuit then reduces to that shown in Fig. 9.72(a), generating a ramp output with a slope equal to I_{SS}/C_L (if the channel-length modulation of M_4 and the current drawn by $R_1 + R_2$ are neglected). Note that so long as M_2 remains off, the feedback loop is broken and the current charging C_L is constant and independent of the input level. As V_{out} rises, V_X eventually approaches V_{in} , M_2 turns on, and the circuit returns to linear operation.



In Fig. 9.71, slewing occurs for falling edges at the input as well. If the input drops so much that M_1 turns off, then the circuit is simplified as in Fig. 9.72(b), discharging C_L by a current approximately equal to I_{SS} . After V_{out} decreases sufficiently, the difference between V_X and V_{in} is small enough to allow M_1 to turn on, leading to linear behavior thereafter.

The foregoing observations explain why slewing is a nonlinear phenomenon. If the input amplitude, say, doubles, the output level does not double at *all* points because the ramp exhibits a slope independent of the input.

Power Supply Rejection

As with other analog circuits, op amps are often supplied from noisy lines and must therefore “reject” the noise adequately. For this reason, it is important to understand how noise on the supply manifests itself at the output of an op amp.

Let us consider the simple op amp shown in Fig. 9.81, assuming that the supply voltage varies slowly.

If the circuit is perfectly symmetric, $V_{out} = V_X$. Since the diode-connected device “clamps” node X to V_{DD} , V_X and hence V_{out} experience approximately the same change as does V_{DD} . In other words, the gain from V_{DD} to V_{out} is close to unity. The power supply rejection ratio (PSRR) is defined as the gain from the input to the output divided by the gain from the supply to the output. At low frequencies:

$$\text{PSRR} \approx g_{mN}(r_{OP} \parallel r_{ON}) \quad (9.81)$$

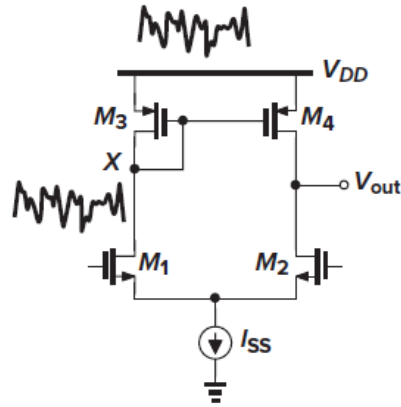


Figure 9.81 Supply rejection of differential pair with active current mirror.

Noise in Op Amps

In low-noise applications, the input-referred noise of op amps becomes critical. We now extend the noise analysis of differential amplifiers in Chapter 7 to more sophisticated topologies. With many transistors in an op amp, it may seem difficult to intuitively identify the dominant sources of noise. A simple rule for inspection is to (mentally) change the gate voltage of each transistor by a small amount and predict the effect at the output.

Let us first consider the telescopic op amp shown in Fig. 9.84. At relatively low frequencies, the cascode devices contribute negligible noise, leaving M_1 – M_2 and M_7 – M_8 as the primary noise sources.

The input-referred noise voltage per unit bandwidth is therefore similar to that in Fig. 7.59(a) and given by

$$\overline{V_n^2} = 4kT \left(2 \frac{\gamma}{g_{m1,2}} + 2 \frac{\gamma g_{m7,8}}{g_{m1,2}^2} \right) + 2 \frac{K_N}{(WL)_{1,2} C_{ox} f} + 2 \frac{K_P}{(WL)_{7,8} C_{ox} f} \frac{g_{m7,8}^2}{g_{m1,2}^2} \quad (9.88)$$

where K_N and K_P denote the $1/f$ noise coefficients of NMOS and PMOS devices, respectively.

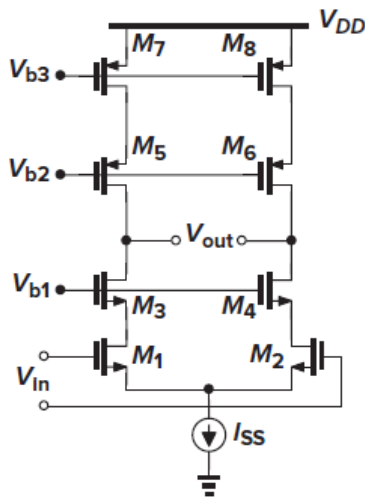
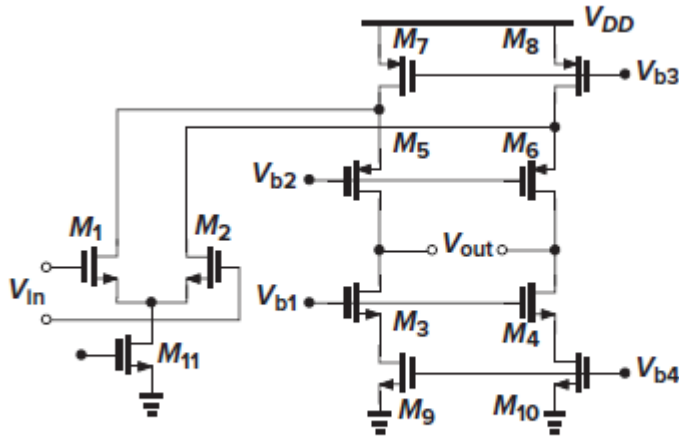
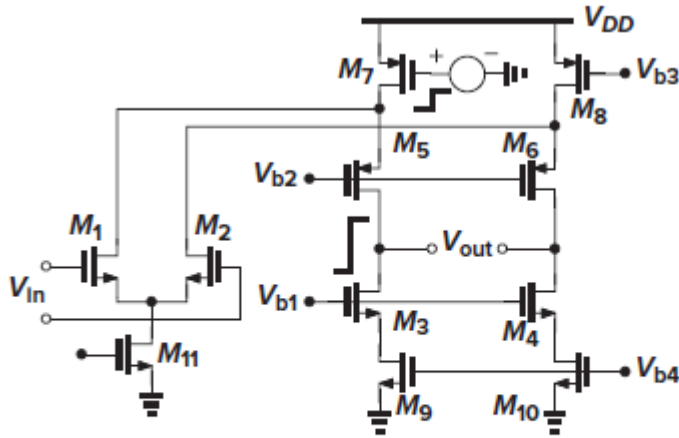


Figure 9.84 Noise in a telescopic op amp.

Next, we study the noise behavior of the folded-cascode op amp of Fig. 9.85(a), considering only thermal noise at this point. Again, the noise of the cascode devices is negligible at low frequencies, leaving M_1 – M_2 , M_7 – M_8 , and M_9 – M_{10} as potentially significant sources. Do both pairs M_7 – M_8 and M_9 – M_{10} contribute noise? Using our simple rule, we change the gate voltage of M_7 by a small amount [Fig. 9.85(b)], noting that the output indeed changes considerably. The same observation applies to M_8 – M_{10} as well. To determine the input-referred thermal noise, we first refer the noise of M_7 – M_8 to the



(a)



(b)

Figure 9.85 Noise in a folded-cascode op amp.

output:

$$\overline{V_{n,out}^2} |_{M7,8} = 2 \left(4kT \frac{\gamma}{g_{m7,8}} g_{m7,8}^2 R_{out}^2 \right) \quad (9.89)$$

where the factor 2 accounts for the (uncorrelated) noise of M_7 and M_8 and R_{out} denotes the open-loop output resistance of the op amp. Similarly,

$$\overline{V_{n,out}^2} |_{M9,10} = 2 \left(4kT \frac{\gamma}{g_{m9,10}} g_{m9,10}^2 R_{out}^2 \right) \quad (9.90)$$

Dividing these quantities by $g_{m1,2}^2 R_{out}^2$ and adding the contribution of M_1 – M_2 , we obtain the overall noise:

$$\overline{V_{n,int}^2} = 8kT \left(\frac{\gamma}{g_{m1,2}} + \gamma \frac{g_{m7,8}}{g_{m1,2}^2} + \gamma \frac{g_{m9,10}}{g_{m1,2}^2} \right) \quad (9.91)$$

The effect of flicker noise can be included in a similar manner (Problem 9.15). Note that the folded-cascode topology potentially suffers from greater noise than its telescopic counterpart. In applications

where flicker noise is critical, we opt for a PMOS-input op amp as PMOS transistors typically exhibit less flicker noise than do NMOS devices.

As observed for the differential amplifiers in Chapter 7, the noise contribution of the PMOS and NMOS current sources *increases* in proportion to their transconductance. This trend results in a tradeoff between output voltage swings and input-referred noise: for a given current, as implied by $g_m = 2I_D/(V_{GS} - V_{TH})$, if the overdrive voltage of the current sources is minimized to allow large swings,

then their transconductance is maximized.

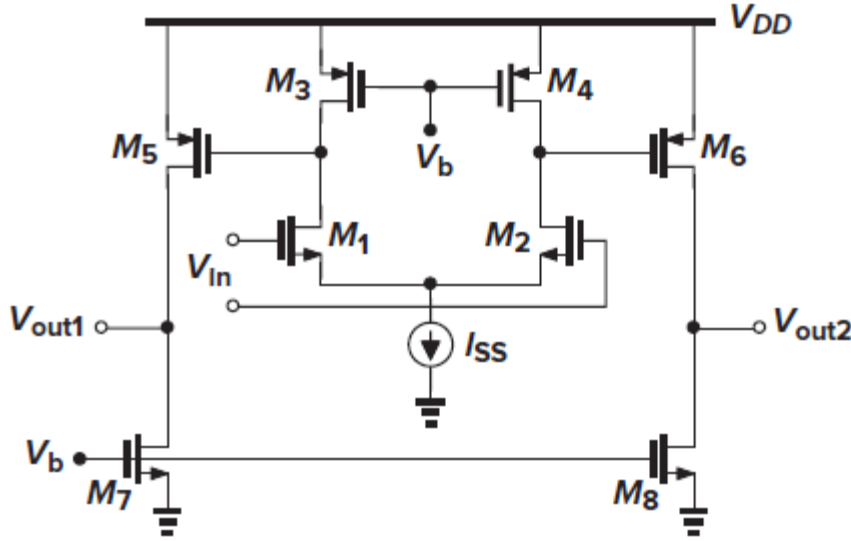


Figure 9.86 Noise in a two-stage op amp.

As another case, we calculate the input-referred thermal noise of the two-stage op amp shown in Fig. 9.86. Beginning with the second stage, we note that the noise current of M_5 and M_7 flows through $r_{O5}r_{O7}$. Dividing the resulting output noise voltage by the total gain, $g_{m1}(r_{O1}r_{O3}) \times g_{m5}(r_{O5}r_{O7})$, and doubling the power, we obtain the input-referred contribution of M_5 – M_8 :

$$\overline{V_n^2}|_{M_5-8} = 2 \times 4kT\gamma(g_{m5} + g_{m7})(r_{O5}\|r_{O7})^2 \frac{1}{g_{m1}^2(r_{O1}\|r_{O3})^2 g_{m5}^2(r_{O5}\|r_{O7})^2} \quad (9.92)$$

$$= 8kT\gamma \frac{g_{m5} + g_{m7}}{g_{m1}^2 g_{m5}^2 (r_{O1}\|r_{O3})^2} \quad (9.93)$$

The noise due to M_1 – M_4 is simply equal to

$$\overline{V_n^2}|_{M_1-4} = 2 \times 4kT\gamma \frac{g_{m1} + g_{m3}}{g_{m1}^2} \quad (9.94)$$

It follows that

$$\overline{V_{n,tot}^2} = 8kT\gamma \frac{1}{g_{m1}^2} \left[g_{m1} + g_{m3} + \frac{g_{m5} + g_{m7}}{g_{m5}^2 (r_{O1}\|r_{O3})^2} \right] \quad (9.95)$$

Note that the noise resulting from the second stage is usually negligible because it is divided by the gain of the first stage when referred to the main input.