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CEC334 Analog IC design
UNIT-I Single stage amplifier

1. Explain in detail about the Common-Source Stage with Resistive Load with neat diagram

By virtue of its transconductance, a MOSFET converts changes in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage. Shown in Fig. 3.4(a), the common-source stage performs such an operation. We study both the large-signal and the small-signal behavior of the circuit. Note that the input impedance of the circuit is very high at low frequencies. If the input voltage increases from zero, M_1 is off and $V_{out} = V_{DD}$ [Fig. 3.4(b)]. As V_{in} approaches V_{TH} , M_1 begins to turn on, drawing current from R_D and lowering V_{out} . Transistor M_1 turns on in saturation regardless of the values of V_{DD} and R_D .

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \quad (3.3)$$

where channel-length modulation is neglected. With further increase in V_{in} , V_{out} drops more, and the transistor continues to operate in saturation until V_{in} exceeds V_{out} by V_{TH} [point A in Fig. 3.4(b)]. At this point,

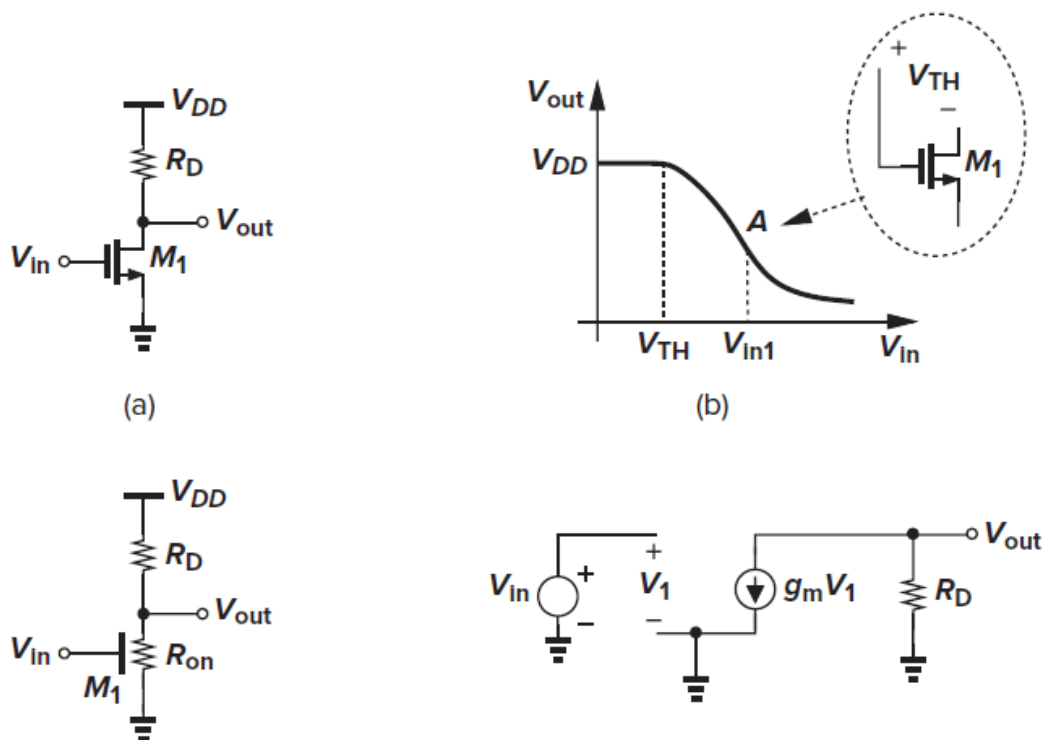
$$V_{in1} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2 \quad (3.4)$$

from which $V_{in1} - V_{TH}$ and hence V_{out} can be calculated.

For $V_{in} > V_{in1}$, M_1 is in the triode region:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [2(V_{in} - V_{TH})V_{out} - V_{out}^2] \quad (3.5)$$

Figure 3.4 (a) Common-source stage, (b) input-output characteristic, (c) equivalent circuit in the deep triode region, and (d) small-signal model for the saturation region.



If V_{in} is high enough to drive M_1 into the deep triode region, $V_{out} \approx 2(V_{in} - V_{TH})$, and, from the equivalent circuit of Fig. 3.4(c),

$$V_{out} = V_{DD} \frac{R_{on}}{R_{on} + R_D} \quad (3.6)$$

$$= \frac{V_{DD}}{1 + \mu_n C_{ox} \frac{W}{L} R_D (V_{in} - V_{TH})} \quad (3.7)$$

Since the transconductance drops in the triode region, we usually ensure that $V_{out} > V_{in} - V_{TH}$, and hence the current operates to the left of point A in Fig. 3.4(b). Using (3.3) as the input-output characteristic and viewing its slope as the small-signal gain, we have

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} \quad (3.8)$$

$$= -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH}) \quad (3.9)$$

$$= -g_m R_D \quad (3.10)$$

This result can be directly derived from the observation that M_1 converts an input voltage change V_{in} to a drain current change $g_m V_{in}$, and hence an output voltage change $-g_m R_D V_{in}$. The small-signal model of Fig. 3.4(d) yields the same result: $V_{out} = -g_m V_{in} R_D = -g_m R_D V_{in}$.

Even though derived for small-signal operation, the equation $A_v = -g_m R_D$ predicts certain effects if the circuit senses a *large* signal swing. Since g_m itself varies with the input signal according to $g_m = \mu_n C_{ox} (W/L)(V_{GS} - V_{TH})$, the gain of the circuit changes substantially if the signal is large. In other words, if the gain of the circuit *varies* significantly with the signal swing, then the circuit operates in the large-signal mode. The dependence of the gain upon the signal level leads to nonlinearity usually an undesirable effect.

A key result here is that to minimize the nonlinearity, the gain equation must be a weak function of signal-dependent parameters such as g_m .

2. Explain in detail about the CS Stage with Diode-Connected Load

A MOSFET can operate as a small-signal resistor if its gate and drain are shorted [Fig. 3.10(a)]. Called a “diode-connected” device in analogy with its bipolar counterpart, this configuration exhibits small-signal behavior similar to that of two-terminal resistor. Note that the transistor is always in saturation because the drain and the gate have the same potential. Using the small-signal equivalent shown in Fig. 3.10(b) to obtain the impedance of the device, we write $V_1 = V_X$ and $I_X = V_X / r_O + g_m V_X$. That is, the impedance of the diode is simply equal to $V_X / I_X = (1/g_m)_{r_O} \approx 1/g_m$. If body effect exists, we can use the circuit in Fig. 3.11 to write $V_1 = -V_X$, $V_{bs} = -V_X$, and

$$(g_m + g_{mb})V_X + \frac{V_X}{r_O} = I_X \quad (3.21)$$

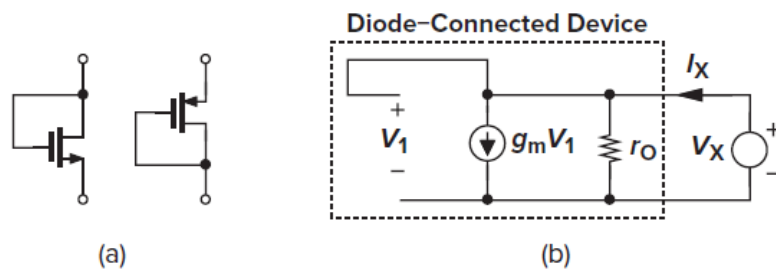


Figure 3.10 (a) Diode-connected NMOS and PMOS devices; (b) small-signal equivalent circuit.

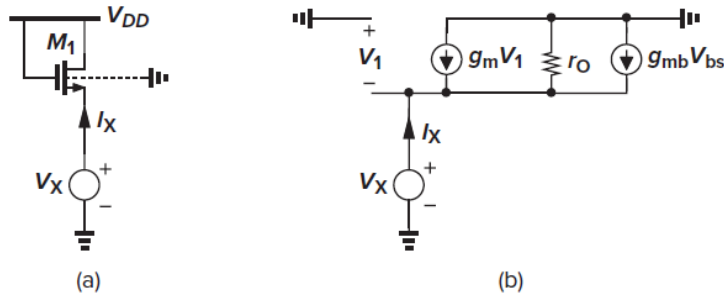


Figure 3.11 (a) Arrangement for measuring the equivalent resistance of a diode-connected MOSFET; (b) small-signal equivalent circuit.

It follows that

$$\frac{V_X}{I_X} = \frac{1}{g_m + g_{mb} + r_O^{-1}} \quad (3.22)$$

$$= \frac{1}{g_m + g_{mb}} \parallel r_O \quad (3.23)$$

$$\approx \frac{1}{g_m + g_{mb}} \quad (3.24)$$

In the general case, $V_X/I_X = (1/g_m) \parallel r_O \parallel (1/g_{mb})$. Interestingly, the impedance seen at the source of M_1 is *lower* when body effect is included.

3. Explain in detail about the CS Stage with Active Load

In the amplifier topology of Fig. 3.19(b), the PMOS device serves as a constant current source. Is it possible for M_2 to operate as an *amplifying* device? Yes; we can apply the input signal to the gate of M_2 as well [Fig. 3.20(a)], converting it to an “active” load. The reader may recognize this topology as a CMOS inverter. Suppose both transistors are in saturation and V_{in} rises by $_V_0$. Two changes now occur: (a) I_{D1} increases, pulling V_{out} lower, and (b) M_2 injects less current into the output node, allowing V_{out} to drop. The two changes thus *enhance* each other, leading to a greater voltage gain. Equivalently, as seen in Fig. 3.20(b), the two transistors operate in parallel and collapse into one as illustrated in Fig. 3.20(c).

It follows that $-(g_{m1} + g_{m2})V_{in}(r_{O1} \parallel r_{O2}) = V_{out}$, and hence

$$A_v = -(g_{m1} + g_{m2})(r_{O1} \parallel r_{O2})$$

Compared to the amplifier of Fig. 3.19(b), this circuit exhibits the same output resistance, $r_{O1} \parallel r_{O2}$, but a higher transconductance. This topology is also called a “complementary CS stage.”

The amplifier of Fig. 3.20(a) must deal with two critical issues. First, the bias current of the two transistors is a strong function of PVT. In particular, since $V_{GS1} + |V_{GS2}| = V_{DD}$, variations in V_{DD} or the threshold voltages directly translate to changes in the drain currents. Second, the circuit *amplifies*

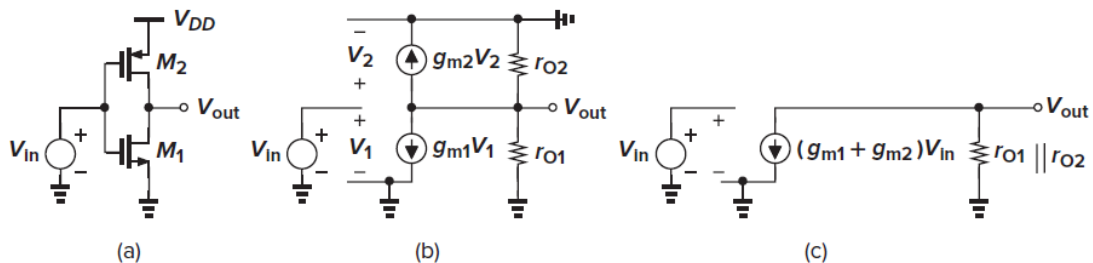


Figure 3.20 (a) CS stage with active load, (b) small-signal model, and (c) simplified model.

supply voltage variations (“supply noise”)! To understand this point, consider the arrangement depicted in Fig. 3.21, where V_B is a bias voltage to place M_1 and M_2 in saturation. In Problem 3.31, we prove that the small-signal gain from V_{DD} to V_{out} is given by

$$\frac{V_{out}}{V_{DD}} = \frac{g_{m2}r_{O2} + 1}{r_{O2} + r_{O1}} r_{O1} \quad (3.49)$$

$$= \left(g_{m2} + \frac{1}{r_{O2}} \right) (r_{O1} \parallel r_{O2}) \quad (3.50)$$

about half of the A_v found above. These issues are addressed in Chapter 5.

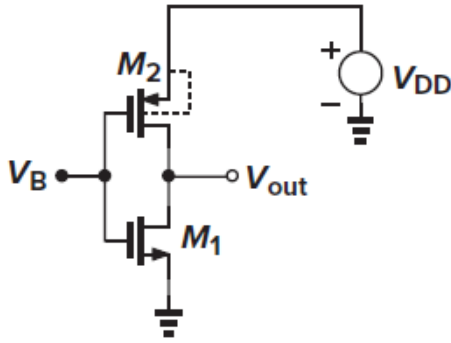


Figure 3.21 Arrangement for studying supply sensitivity of CS stage with active load.

4. Explain in detail about the Source follower

common-source stage indicates that, to achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible. If such a stage is to drive a low-impedance load, then a “buffer” must be placed after the amplifier so as to drive the load with negligible reduction in gain. The source follower (also called the “common-drain” stage) can operate as a voltage buffer.

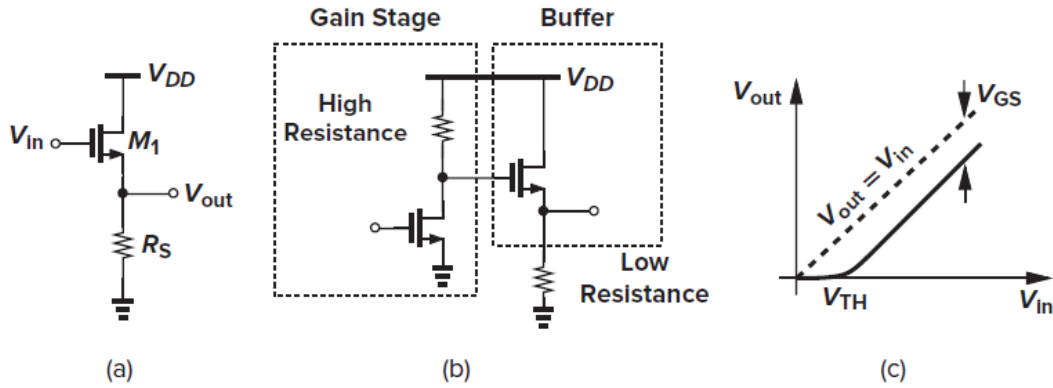


Figure 3.34 (a) Source follower, (b) example of its role as a buffer, and (c) its input-output characteristic.

Illustrated in Fig. 3.34(a), the source follower senses the signal at the gate, while presenting a high input impedance, and drives the load at the source, allowing the source potential to “follow” the gate voltage. Figure 3.34(b) depicts how the circuit can be used to drive a low resistance without degrading the voltage gain of a CS stage. Beginning with the large-signal behavior of the source follower, we note that for $V_{in} < V_{TH}$, M_1 is off and $V_{out} = 0$. As V_{in} exceeds V_{TH} , M_1 turns on in saturation (why?) and I_{D1} flows through R_S [Fig. 3.34(c)]. As V_{in} increases further, V_{out} follows the input with a difference (level shift) equal to V_{GS} . We can express the input-output characteristic as

$$\frac{1}{2}\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})^2 R_S = V_{out} \quad (3.82)$$

where channel-length modulation is neglected. Let us calculate the small-signal gain of the circuit by differentiating both sides of (3.82) with respect to V_{in} :

$$\frac{1}{2}\mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH} - V_{out}) \left(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}\right) R_S = \frac{\partial V_{out}}{\partial V_{in}} \quad (3.83)$$

Since $\partial V_{TH} / \partial V_{in} = (\partial V_{TH} / \partial V_{SB})(\partial V_{SB} / \partial V_{in}) = \eta \partial V_{out} / \partial V_{in}$,

$$\frac{\partial V_{out}}{\partial V_{in}} = \frac{\mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out}) R_S}{1 + \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out}) R_S (1 + \eta)} \quad (3.84)$$

Also, note that

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out}) \quad (3.85)$$

Consequently,

$$A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \quad (3.86)$$

The same result is more easily obtained with the aid of a small-signal equivalent circuit. From Fig. 3.35, we have $V_{in} - V_1 = V_{out}$, $V_{bs} = -V_{out}$, and $g_m V_1 - g_{mb} V_{out} = V_{out} / R_S$. Thus, $V_{out} / V_{in} = g_m R_S / [1 + (g_m + g_{mb}) R_S]$.

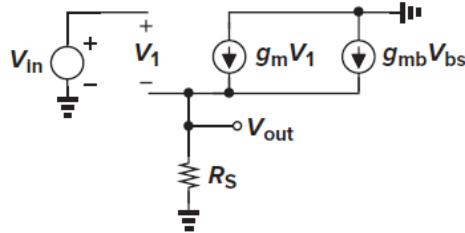


Figure 3.35 Small-signal equivalent circuit of source follower.

Sketched in Fig. 3.36 vs. V_{in} , the voltage gain begins from zero for $V_{in} \approx V_{TH}$ (that is, $g_m \approx 0$) and monotonically increases. As the drain current and g_m increase, A_v approaches $g_m / (g_m + g_{mb}) = 1 / (1 + \eta)$. Since η itself slowly decreases with V_{out} , A_v would eventually become equal to unity, but for typical allowable source-bulk voltages, η remains greater than roughly 0.2.

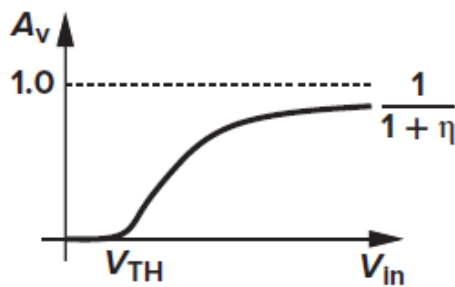


Figure 3.36 Voltage gain of source follower versus input voltage.

An important result of (3.86) is that even if $R_S = \infty$, the voltage gain of a source follower is not equal to one (unless body effect is removed as explained later). We return to this point later. Note that M_1 in Fig. 3.34(a) remains in saturation if V_{in} does not exceed $V_{DD} + V_{TH}$.

In the source follower of Fig. 3.34(a), the drain current of M_1 heavily depends on the input dc level.

For example, if V_{in} changes from 0.7 V to 1 V, I_D may increase by a factor of 2, and hence $V_{GS} - V_{TH}$ by $\sqrt{2}$.

2. Even if V_{TH} is relatively constant, the increase in V_{GS} means that $V_{out} (= V_{in} - V_{GS})$ does not follow V_{in} faithfully, thereby incurring nonlinearity. To alleviate this issue, the resistor can be replaced by a constant current source as shown in Fig. 3.37(a). The current source itself is implemented as an NMOS transistor operating in the saturation region [Fig. 3.37(b)].

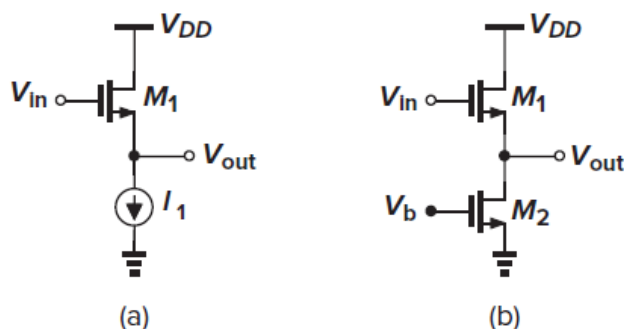


Figure 3.37 Source follower using (a) an ideal current source, and (b) an NMOS transistor as a current source.

5. Explain in detail about the Common Gate Amplifier

In common-source amplifiers and source followers, the input signal is applied to the gate of a MOSFET. It is also possible to apply the signal to the source terminal. Shown in Fig. 3.48(a), a common-gate (CG) stage senses the input at the source and produces the output at the drain. The gate is connected to a dc voltage to establish proper operating conditions. Note that the bias current of M_1 flows through the input signal source. Alternatively, as depicted in Fig. 3.48(b), M_1 can be biased by a constant current source, with the signal capacitively coupled to the circuit.

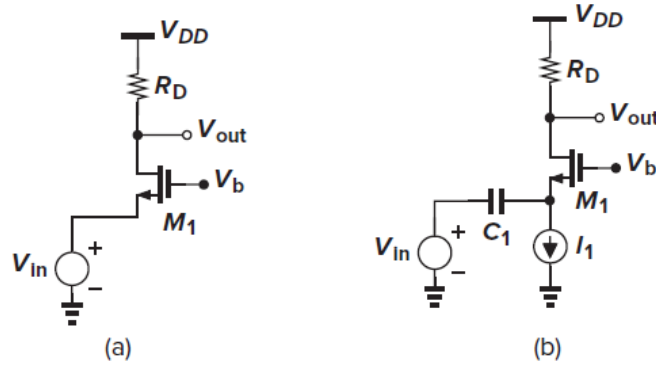


Figure 3.48 (a) Common-gate stage with direct coupling at input; (b) CG stage with capacitive coupling at input.

Chapter 3 Single-Stage Amplifiers

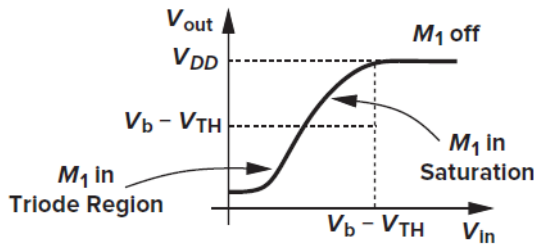


Figure 3.49 Common-gate input-output characteristic.

We first study the large-signal behavior of the circuit in Fig. 3.48(a). For simplicity, let us assume that V_{in} decreases from a large positive value. Also, $\lambda = 0$. For $V_{in} \geq V_b - V_{TH}$, M_1 is off and $V_{out} = V_{DD}$. For lower values of V_{in} , we can write

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 \quad (3.102)$$

if M_1 is in saturation. As V_{in} decreases, so does V_{out} , eventually driving M_1 into the triode region if

$$V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH} \quad (3.103)$$

The input-output characteristic is shown in Fig. 3.49, illustrating a case in which M_1 enters the triode region as V_{in} decreases. In the region where M_1 is saturated, we can express the output voltage as

$$V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D \quad (3.104)$$

obtaining a small-signal gain of

$$\frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W}{L} (V_b - V_{in} - V_{TH}) \left(-1 - \frac{\partial V_{TH}}{\partial V_{in}} \right) R_D \quad (3.105)$$

Since $\partial V_{TH} / \partial V_{in} = \partial V_{TH} / \partial V_{SB} = \eta$, we have

$$\frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} R_D (V_b - V_{in} - V_{TH}) (1 + \eta) \quad (3.106)$$

$$= g_m (1 + \eta) R_D \quad (3.107)$$

For a given bias current and supply voltage (i.e., a given power budget), how do we maximize the voltage gain of a CG stage? We can increase g_m by widening the input device, eventually reaching

subthreshold operation [$g_m \approx I_D / (\xi V_T)$] (why?), and/or we can increase R_D and, inevitably, the dc drop across it. We must bear in mind that the minimum allowable level of V_{out} in Fig. 3.48(b) is equal to $V_{GS} - V_{TH} + V_{I1}$, where V_{I1} denotes the minimum voltage required by I_1 .

6. Explain in detail about the Cascode stage amplifier

The cascade of a CS stage and a CG stage is called a “cascode”⁴ topology, providing many useful properties. Figure 3.59 shows the basic configuration: M_1 generates a small-signal drain current proportional to the small-signal input voltage, V_{in} , and M_2 simply routes the current to R_D . We call M_1 the input device and M_2 the cascode device. Note that in this example, M_1 and M_2 carry equal bias and signal currents. As we describe the attributes of the circuit in this section, many advantages of the cascode topology over a simple common-source stage become evident. This circuit is also known as the “telescopic” cascode.

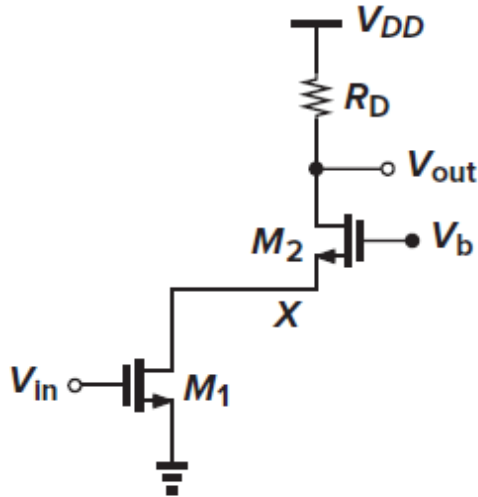


Figure 3.59 Cascode stage.

Before delving into our analysis, it is instructive to explore the circuit qualitatively. We wish to know what happens if the value of V_{in} or V_b changes by a small amount. Assume that both transistors are in saturation and $\lambda = \gamma = 0$. If V_{in} rises by ΔV , then I_{D1} increases by $g_{m1} \Delta V$. This change in current flows through the impedance seen at X, i.e., the impedance seen at the source of M_2 , which is equal to $1/g_{m2}$. Thus, V_X falls by an amount given by $g_{m1} \Delta V \cdot (1/g_{m2})$ [Fig. 3.60(a)]. The change in I_{D1} also flows through R_D , producing a drop of $g_{m1} \Delta V R_D$ in V_{out} —just as in a simple CS stage.

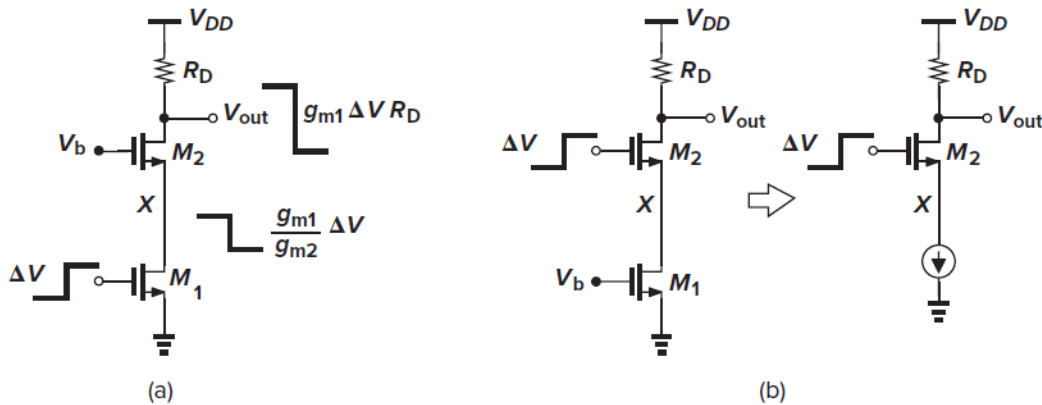


Figure 3.60 Cascode stage sensing a signal at the gate of (a) an input device and (b) a cascode device.

Now, consider the case where V_{in} is fixed and V_b increases by ΔV . Since V_{GS1} is constant and $r_{o1} = \infty$, we simplify the circuit as shown in Fig. 3.60(b). How do V_X and V_{out} change here? As far as node X is concerned, M_2 operates as a *source follower* because it senses an input, ΔV , at its gate and generates an output at X. With $\lambda = \gamma = 0$, the small-signal voltage gain of the follower is equal to unity, regardless of the value of R_D (why?). Thus, V_X rises by ΔV . On the other hand, V_{out} does *not* change because I_{D2} is equal to I_{D1} and hence remains *constant*. We say that the voltage gain from V_b to V_{out} is zero in this case.

Let us now study the bias conditions of the cascode, still assuming that $\lambda = \gamma = 0$. For M_1 to operate in saturation, we must have $V_X \geq V_{in} - V_{TH1}$. If M_1 and M_2 are both in saturation, M_2 operates as a source follower and V_X is determined primarily by V_b : $V_X = V_b - V_{GS2}$. Thus, $V_b - V_{GS2} \geq V_{in} - V_{TH1}$,

and hence $V_b > V_{in} + V_{GS2} - V_{TH1}$ (Fig. 3.61). For M_2 to be saturated, $V_{out} \geq V_b - V_{TH2}$; that is,

$$V_{out} \geq V_{in} - V_{TH1} + V_{GS2} - V_{TH2} \quad (3.124)$$

$$= (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \quad (3.125)$$

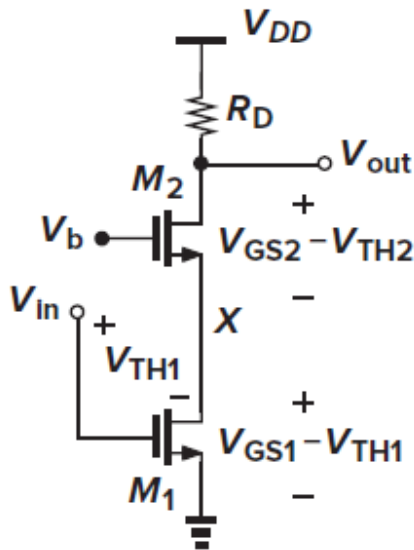


Figure 3.61 Allowable voltages in cascode stage.

if V_b is chosen to place M_1 at the edge of saturation. Consequently, the minimum output level for which both transistors operate in saturation is equal to the overdrive voltage of M_1 plus that of M_2 . In other words, addition of M_2 to the circuit reduces the output voltage swing by at least the overdrive voltage of M_2 . We say that M_2 is “stacked” on top of M_1 . We also loosely say that the minimum output voltage is equal to two overdrives or $2V_{D,sat}$.

We now analyze the large-signal behavior of the cascode stage shown in Fig. 3.59 as V_{in} goes from zero to V_{DD} . For $V_{in} \leq V_{TH1}$, M_1 and M_2 are off, $V_{out} = V_{DD}$, and $V_X \approx V_b - V_{TH2}$ (if subthreshold conduction is neglected) (Fig. 3.62). As V_{in} exceeds V_{TH1} , M_1 begins to draw current, and V_{out} drops. Since I_{D2} increases, V_{GS2} must increase as well, causing V_X to fall. As V_{in} assumes sufficiently large values, two effects can occur: (1) V_X drops below V_{in} by V_{TH1} , forcing M_1 into the triode region; (2) V_{out} drops below V_b by V_{TH2} , driving M_2 into the triode region. Depending on the device dimensions and the values of R_D and V_b , one effect may occur before the other. For example, if V_b is relatively low, M_1 may enter the triode region first. Note that if M_2 goes into the deep triode region, V_X and V_{out} become nearly equal.

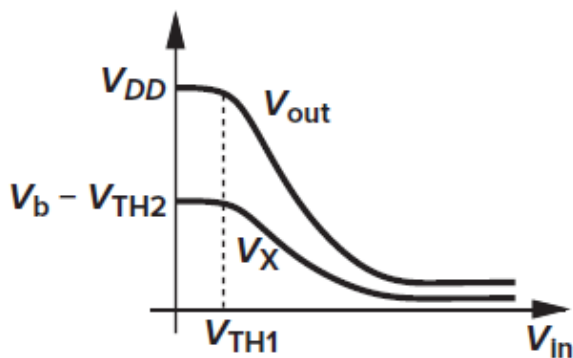


Figure 3.62 Input-output characteristic of a cascode stage.

Let us now consider the small-signal characteristics of a cascode stage, assuming that both transistors operate in saturation. If $\lambda = 0$, the voltage gain is equal to that of a common-source stage because the drain current produced by the input device must flow through the cascode device. Illustrated in the equivalent circuit of Fig. 3.63, this result is independent of the transconductance and body effect of M_2 . It can also be verified using $A_v = -G_m R_{out}$.

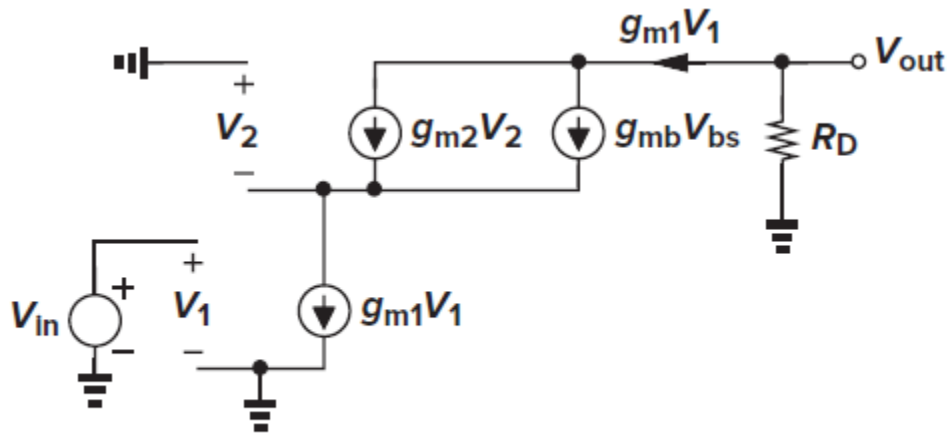


Figure 3.63 Small-signal equivalent circuit of cascode stage.

Output Resistance An important property of the cascode structure is its high output impedance. As illustrated in Fig. 3.65, for calculation of R_{out} , the circuit can be viewed as a common-source stage with a degeneration resistor equal to r_{o1} . Thus, from (3.66),

$$R_{out} = [1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2} \quad (3.128)$$

Assuming $g_{mro} \gg 1$, we have $R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$. That is, M_2 boosts the output impedance of M_1 by a factor of $(g_{m2} + g_{mb2})r_{o2}$. As shown in Fig. 3.66, cascoding can be extended to three or more stacked devices to achieve a higher output impedance, but the required additional voltage

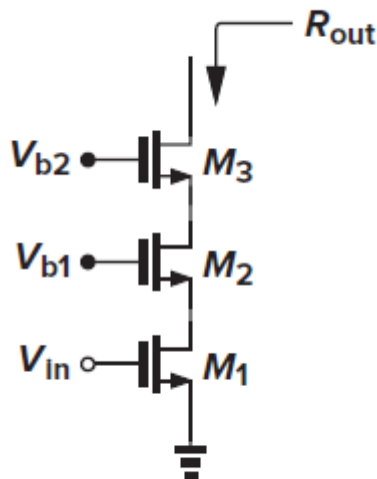


Figure 3.66 Triple cascode.

headroom makes such configurations less attractive. For example, the minimum output voltage of a triple cascode is equal to the sum of three overdrive voltages.

To appreciate the utility of a high output impedance, recall from the lemma in Sec. 3.3.3 that the voltage gain can be written as $-G_m R_{out}$. Since G_m is typically determined by the transconductance of a transistor, e.g., M_1 in Fig. 3.59, and hence bears trade-offs with the bias current and device capacitances, it is desirable to increase the voltage gain by maximizing R_{out} . Shown in Fig. 3.67 is an example.

If both M_1 and M_2 operate in saturation, then $G_m \approx g_{m1}$ and $R_{out} \approx (g_{m2} + g_{mb2})r_{o2}r_{o1}$, yielding

$A_v = (g_{m2} + g_{mb2})r_{o2}g_{m1}r_{o1}$. Thus, the maximum voltage gain is roughly equal to the *square* of the intrinsic gain of the transistors.

7. Explain in detail about the Folded cascode amplifier.

The idea behind the cascode structure is to convert the input voltage to a current and apply the result to a common-gate stage. However, the input device and the cascode device need not be of the same type. For example, as depicted in Fig. 3.74(a), a PMOS-NMOS combination performs the same function. In order to bias M_1 and M_2 , a current source must be added as in Fig. 3.74(b). Note that $|I_{D1}| + I_{D2}$ is equal to I_1 and hence constant. The small-signal operation is as follows. If V_{in} becomes more positive, $|I_{D1}|$ decreases, forcing I_{D2} to increase and hence V_{out} to drop. The voltage gain and output impedance of the circuit can be obtained as calculated for the NMOS-NMOS cascode of Fig. 3.59. Shown in Fig. 3.74(c) is an NMOS-PMOS cascode. The advantages and disadvantages of these types will be explained later.

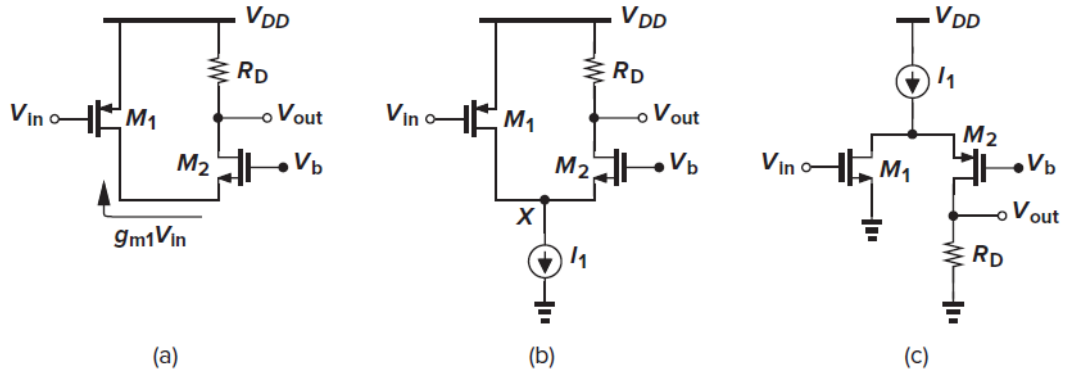


Figure 3.74 (a) Simple folded cascode; (b) folded cascode with proper biasing; (c) folded cascode with NMOS input.

The structures of Figs. 3.74(b) and (c) are called “folded cascode” stages because the small-signal current is “folded” up [in Fig. 3.74(b)] or down [in Fig. 3.74(c)]. We should mention as a point of contrast that the bias current of M_1 in Fig. 3.70 flows through M_2 , i.e., it is “reused,” whereas those of M_1 and M_2 in Fig. 3.74(b) add up to I_1 . Thus, the total bias current in this case must be higher than that in Fig. 3.70 to achieve a comparable performance. It is instructive to examine the large-signal behavior of a folded-cascode stage. Suppose that in Fig. 3.74(b), V_{in} decreases from V_{DD} to zero. For $V_{in} > V_{DD} - |V_{TH1}|$, M_1 is off and M_2 carries all of I_1 , yielding $V_{out} = V_{DD} - I_1 R_D$. For $V_{in} < V_{DD} - |V_{TH1}|$, M_1 turns on in saturation, giving

$$I_{D2} = I_1 - \frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2 \quad (3.143)$$

As V_{in} drops, I_{D2} decreases further, falling to zero if $I_{D1} = I_1$. This occurs at $V_{in} = V_{in1}$ if

$$\frac{1}{2} \mu_p C_{ox} \left(\frac{W}{L} \right)_1 (V_{DD} - V_{in1} - |V_{TH1}|)^2 = I_1 \quad (3.144)$$

Thus,

$$V_{in1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox} (W/L)_1}} - |V_{TH1}| \quad (3.145)$$

If V_{in} falls below this level, I_{D1} tends to be greater than I_1 , and M_1 enters the triode region so as to ensure $I_{D1} = I_1$. The result is plotted in Fig. 3.75. The reader is encouraged to determine the input voltage at which $|I_{D1}| = I_{D2}$.

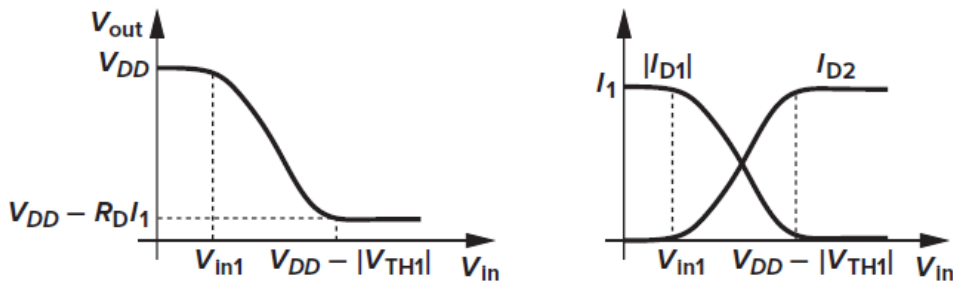


Figure 3.75 Large-signal characteristics of folded cascode.

In order to achieve a high voltage gain, the load of a folded cascode can be implemented as a cascode itself (Fig. 3.77). This structure is studied more extensively in Chapter 9.

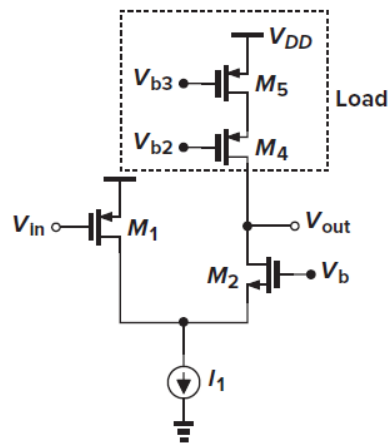


Figure 3.77 Folded cascode with cascode load.

To *increase* the output resistance of voltage amplifiers so as to obtain a high gain. This may seem to make the speed of the circuit quite susceptible to the load capacitance.